MOTOROLA

# GM1200E

# Mobile Radio

## Detailed Service Manual

**68P64115B15**

**European Publications Department (RPG) Fleet, Hampshire, England**
**Issue: July 1998**

# CAUTION

## ELECTROSTATIC SENSITIVE DEVICES

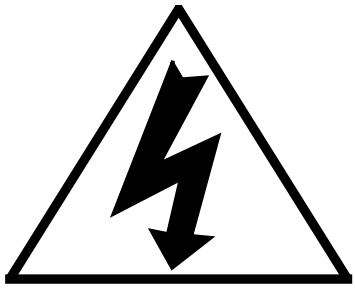
PRECAUTIONS SHOULD BE TAKEN TO MINIMIZE THE RISK OF DAMAGE BY ELECTROSTATIC DISCHARGE TO ELECTROSTATIC SENSITIVE DEVICES (ESDs).

ANY DEVICES EMPLOYING METAL OXIDE SILICON (MOS) TECHNOLOGY ARE PARTICULARLY SUSCEPTIBLE.

CIRCUIT DIAGRAMS MARKED WITH THE ABOVE SYMBOL INDICATE ELECTRONIC CIRCUITS (PECs) FOR WHICH ESD HANDLING PRECAUTIONS ARE NECESSARY.

THE USER SHOULD REFER TO BS5783, 1984: HANDLING OF ELECTROSTATIC SENSITIVE DEVICES. THIS BRITISH STANDARD SUPERSEDES DEF STAN 59-98, ISSUE 2.

# WARNING



## SAFETY WARNINGS

THE ELECTRICAL POWER USED IN THIS EQUIPMENT IS AT A VOLTAGE HIGH ENOUGH TO ENDANGER LIFE.

BEFORE CARRYING OUT MAINTENANCE OR REPAIR, PERSONS CONCERNED MUST ENSURE THAT THIS EQUIPMENT IS ISOLATED FROM THE ELECTRICAL SUPPLY AND TESTS ARE MADE TO ENSURE THAT ISOLATION IS COMPLETE.

WHEN THE SUPPLY CANNOT BE ISOLATED, MAINTENANCE AND REPAIR MUST BE UNDERTAKEN BY PERSONS WHO ARE FULLY AWARE OF THE DANGERS INVOLVED AND WHO HAVE TAKEN ADEQUATE PRECAUTIONS TO PROTECT THEMSELVES.

COMPONENTS CONTAINING BERYLLIUM OXIDE ARE USED IN THIS EQUIPMENT. DUST FROM THIS MATERIAL IS A HEALTH HAZARD IF INHALED OR ALLOWED TO COME INTO CONTACT WITH THE SKIN.

GREAT CARE MUST BE TAKEN WHEN HANDLING THESE COMPONENTS WHICH MUST NOT BE BROKEN OR SUBJECTED TO EXCESSIVE HEATING. DEFECTIVE COMPONENTS MUST BE DISPOSED OF IN ACCORDANCE WITH CURRENT INSTRUCTIONS.

LEAD ACID BATTERIES MAY BE FITTED AS THE STANDBY BATTERY. CARE MUST BE TAKEN WHEN REMOVING OR INSTALLING THESE BATTERIES TO:

1. ENSURE THAT THE TERMINALS ARE NOT SHORTED TOGETHER.

2. PREVENT SPILLAGE OF THE CORROSIVE ELECTROLYTE.

# Detailed Service Manual

## Contents

Chapter

# Chapter 1

## Introduction

## Table of Contents

# 1.0 Introduction

This chapter outlines the scope and use of the detailed service manual and provides an overview of the warranty and service support.

# 2.0 Scope of Manual

This manual is intended for use by experienced technicians familiar with similar types of equipment. It contains level 3 service information required for the equipment described and is current as of the printing date. Changes which occur after the printing date maybe incorporated by a complete Detailed Service Manual revision or alternatively as additions, for example, to Band Specific information.

# 3.0 How to Use This Manual

The detailed service manual contain an introductory chapter giving information on warranty and support. Chapter 2 contains level 3 service information for the control head . Chapter 3 details level 3 service information for the radios in band specific sub-chapters each containing theory of operation and schematics/parts lists. Refer to the Table of Contents for a general overview of the manual.

# 4.0 Warranty and Service Support

Motorola offers long term support for its products. This support includes full exchange and/or repair of the product during the warranty period, and service/ repair or spare parts support out of warranty. Any "return-for-exchange" or "return-for-repair" by an authorised Motorola Dealer must be accompanied by a Warranty Claim Form. Warranty Claim Forms are obtained by contacting an Authorised Motorola Dealer.

## 4.1 Warranty Period

The terms and conditions of warranty are defined fully in the Motorola Dealer or Distributor or Reseller contract. These conditions may change from time to time and the following notes are for guidance purposes only.

In instances where the product is covered under a "return for replacement" or "return for repair" warranty, a check of the product should be performed prior to shipping the unit back to Motorola. To ensure the product has been correctly programmed or has not been subjected to damage outside the terms of the warranty.

Prior to shipping any radios back to the appropriate Motorola warranty depot, please contact Customer Services. All returns must be accompanied by a Warranty Claim Form, available from your Customer Services representative. Products should be shipped back in the original packaging, or correctly packaged to ensure no damage occurs in transit.

## 4.2 After Warranty Period

After Warranty period, Motorola continues to support products in two ways.

Firstly, Motorola's Radio Parts and Service Group (RPSG) offer a repair service to both end users and dealers at competitive prices.

Secondly, RPSG supplies individual parts and modules that can be purchased by dealers who are technically capable of performing fault analysis and repair.

## 4.3 Piece Parts

Some replacement parts, spare parts, and/or product information can be ordered directly. If a complete Motorola part number is assigned to the part, it is available from Motorola Radio Parts and Service Group (RPSG). If a generic part is listed or only a part description is listed, the part is not normally available from Motorola. If a parts list is not included, this generally means that no user-serviceable parts are available for that kit or assembly.

All orders for parts/information should include the complete Motorola identification number. All part orders should be directed to your local RPSG office.

**Head Office**
Motorola G.m.b.H.
European Parts Department
65232 Taunusstein
Germany

## 4.4 Technical Support

Motorola Product Services is available to assist the dealer/distributors in resolving any malfunctions which may be encountered. Initial contact should be by telephone whenever possible. When contacting Motorola Technical Support, be prepared with the product model number and the unit's serial number.

## 4.5 Associated Documentation

| *Publication Number* | *Description* |
|---|---|
| ENLN4051A | GM1200E Product Manual (with Level 1/2 repair information) |
| ENLN4052A | GM1200E Produkthandbuch |
| ENLN4053A | Manuel de Produit GM1200E |
| 68P64117B01 | Shared Mobile Radio Systems (SMR) using MPT1327<br>A System Integrators Cookbook |
| 68P02900X57-A | Data Application Notes for 1200 Series Radios |

# Chapter 2

# Control Head - Level 3 Information

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Chapter

# Chapter 2.1

## Introduction/Theory of Operation

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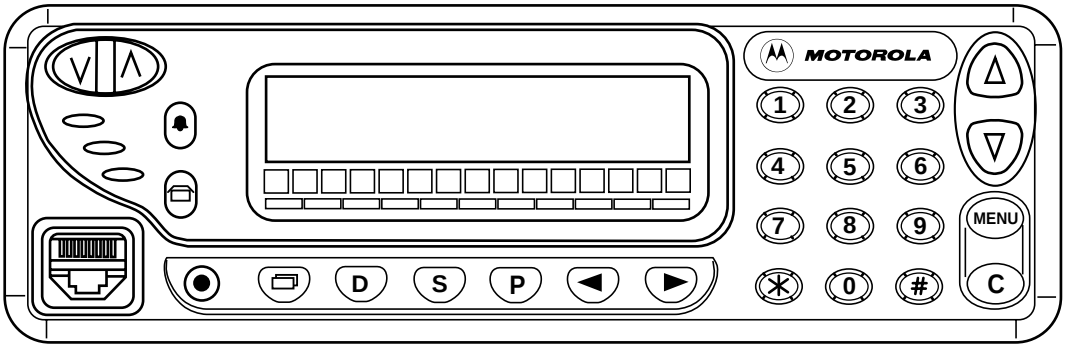
# 1.0 Overview

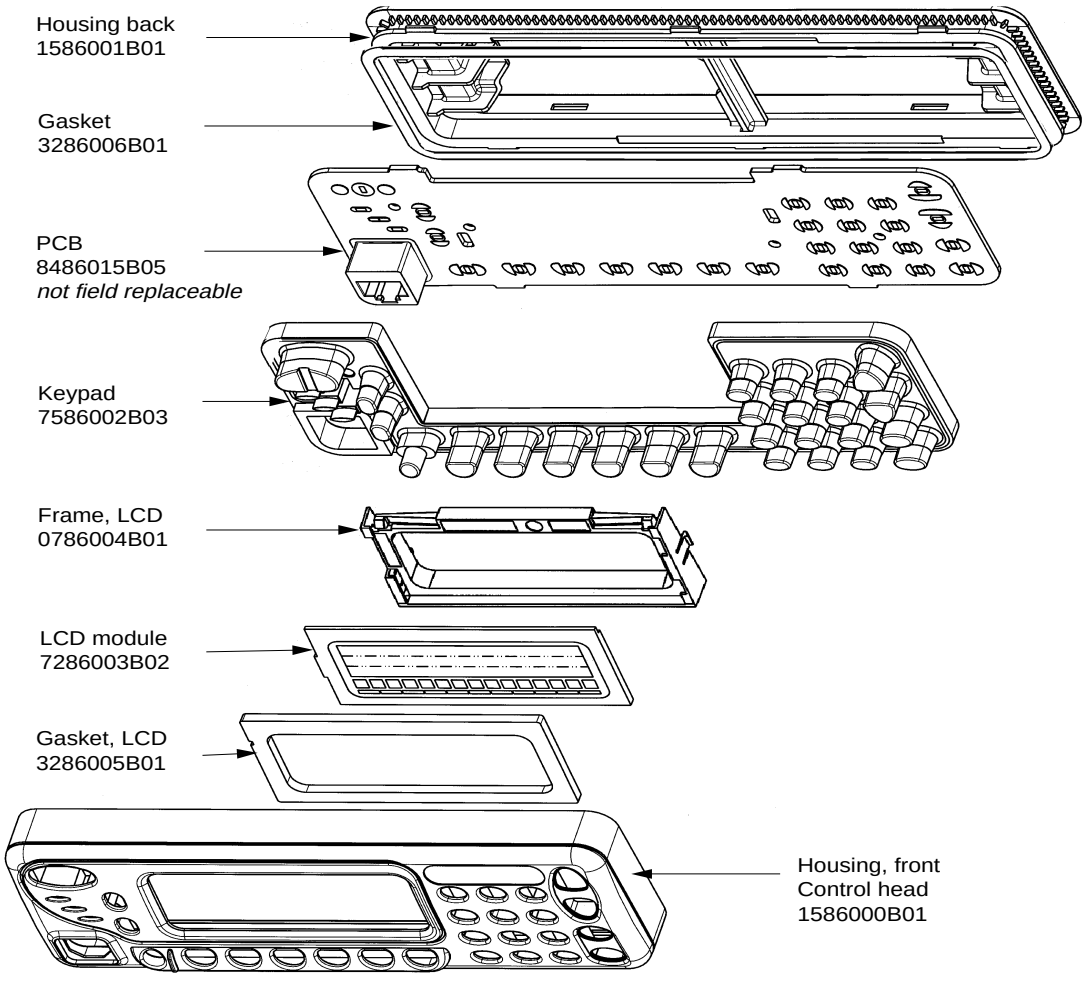
### 128 Channel, Keypad/Display Radio Control Head (Model K6)




The features of the radio control head are as follows:

- ❑ On/Off Button
- ❑ Rocker type Volume Up/Down Control
- ❑ Volume Level Indicators (RSSI)
- ❑ Backlit Liquid Crystal Display (LCD) with display icons to show call progress and status
- ❑ Up/Down scrolling keys for the display
- ❑ Left/Right scrolling keys for the display
- ❑ 3 x 4 CCITT Keypad
- ❑ Clear/Edit Button
- ❑ Status Button
- ❑ Data Button
- ❑ Base Call Button
- ❑ 3 LED's (Red, Yellow and Green)
- ❑ Microphone Socket
- ❑ Menu Button
- ❑ Personality Button
- ❑ Call In Absence Button
- ❑ External Alarm Button

# 2.0 Exploded View Diagram




Control Head Kit GCN6110A

LAPD0008-2

# 3.0 Theory of Operation

## 3.1 General

The control head contains the microphone connector, several buttons to operate the radio, several indicator Light Emitting Diodes (LED) to inform the user about the radio status and a Liquid Crystal Display (LCD) with 19 pre - defined symbols, 11 bars and a 24x120 dot matrix for graphical or alpha - numerical information e.g. channel number, select code, call address name. To control the LEDs and the LCD, and to communicate with the host radio, the control head uses the Motorola 68HC11E9 or 68HC11E20 (dependent on the used character set) microprocessor.

## 3.2 Power Supplies

The power supply to the control head is taken from the host radio FLT A+ voltage via connector J0901 pin 2. The voltage FLT A+ is at battery level and is used for the LEDs, the back light, to power up the radio via On / Off button and to supply the voltage regulator circuit. The regulator circuit provides the stabilized +5 volt which is used for the microprocessor circuit, the display, the display driver and the keypad buttons. The voltage +5V USW also provided by the regulator circuit is used to buffer the internal RAM of the microprocessor (U0901). The regulated +5V taken from the host radio via connector J0901 pin 10 (line +5V SOURCE) is only used to switch on or off the voltage regulator in the control head.

## 3.3 Voltage Regulator Circuit

Voltage regulator U0891 provides 5V for the control head. The supply voltage FLT A+ for the voltage regulator is fed via parallel resistors R0893/4 and dual diode D0891 to pin 8 of U0891. The +5 volt output is switched on and off by the host radio's 5 volt source via line +5V SOURCE and control transistor Q0891. When the host radio is switched off the voltage on line +5V SOURCE is at ground level and switches off transistor Q0891. Pull up resistor R0892 pulls input SHUTDOWN (pin 3) of the voltage regulator U0891 to FLT A+ level and switches off the output of U0891 (pin 1). When the host radio is switched on the voltage on line +5V SOURCE of about +5 volts switches on transistor Q0891 which in turn pulls input SHUTDOWN (pin 3) to ground and switches on the output of U0891. Input and output capacitors (C0892 / C0893 and C0895 - C0896) are used to reduce high frequency noise and provide proper operation during battery transients. Diode D0891 prevents discharge of C0893 by negative spikes on the FLT A+ voltage. This regulator provides a reset output (pin 5) that goes to 0 volts if the regulator output goes out of regulation. This is used to reset the microprocessor (U0901) and the display driver (U0902) to prevent improper operation.

The voltage +5V USW derived from voltage FLT A+ is stabilized using resistor R0896 and diode VR0891 This voltage is used to buffer the microprocessor's internal RAM. C0898 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0892 prevents radio circuitry from discharging this capacitor. The +5V at the second anode of D0892 speeds up charging of C0898 when the host radio is turned on by a high level at the ignition input while the supply voltage is applied to the radio. This prevents the microprocessor from accidently entering bootstrap mode.

## 3.4 Power On / Off

The On/Off button when pressed switches the radio's voltage regulators on by pulling ON OFF CONTROL to high via D0931 and connects the base of Q0932 to FLT A+. This transistor pulls the line ANALOG 3 low to inform the µP that the On/Off button is pressed. If the radio is switched off, the µP will switch it on and vice versa. If the On/Off button is pressed and held while the radio is on, the software detects a low state on line ANALOG 3 and switches the radio off. If the radio is switched on either manually or automatically its +5V source switches on the control head voltage regulator U0891 via line +5 SOURCE and transistor Q0891 and the control head microprocessor starts execution.

## 3.5 Microprocessor Circuit

The control head uses the Motorola 68HC11E9 or 68HC11E20 (dependent on the used character set) microprocessor (μP) (U0901) to control the LEDs, the LCD and to communicate with the host radio. RAM and ROM are contained within the microprocessor itself.

The clock generator for the microprocessor can use two different configurations:

1. The oscillator inside the microprocessor (U0901) along with a 4 MHz ceramic resonator (Y0922) and R0920 generate the clock.

2. The oscillator inside the microprocessor (U0901) along with some external components (C0922-C0924, L0921, R0922, Y0921) generate the 7.9488 MHz clock. Q0921 is used to alter the clock frequency slightly under software control if there is a possibility of harmonics of this clock source interfering with the desired radio receive frequency.

The microprocessor E9/E20 (U0101) contains internal 12 (E9) or 20 (E20) Kbytes ROM, 512 (E9) or 768 (E20) bytes SRAM and 512 bytes EEPROM.

The microprocessor's RAM is always powered to maintain parameters such as the last operating mode. This is achieved by maintaining 5V at U0901-25. Under normal conditions, when the radio is off +5V USW is formed by FLT A+ via D0892. C0898 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0892 prevents radio circuitry from discharging this capacitor.

There are 8 analogue to digital converter ports (A/D) on U0901. They are labelled within the device block as PE0-PE7. These lines sense the voltage level ranging from 0 to 5V of the input line and convert that level to a number ranging from 0 to 255 which can be read by the software to take appropriate action.

U0901-22 is the high reference voltage for the A/D ports on the μP. Resistor R0927 and capacitor C0925 filter the +5V reference. If this voltage is lower than +5V the A/D readings will be incorrect. Likewise U0901-21 is the low reference for the A/D ports. This line is normally tied to ground. If this line is not connected to ground, the A/D readings will be incorrect.

The MODB (U0901-25) input of the μP must be at a logic '1' for it to start executing correctly. The XIRQ (U0901-45) and the IRQ (U0901-46) pins should also be at a logic '1'.

The microprocessor can determine the keypad type used, by reading the voltages at pins 63 and 64. Connections JU0911 and JU0912 are provided by the individual keypads.

Capacitors C0927 and C0928 serve to filter out any AC noise on +5V line at U0901.

## 3.6 Serial Peripheral Interface (SPI)

The host radio (master) communicates to the control head μP (slave) through its SPI port (BUS). This port consists of SPI TRANSMIT DATA (SPI MOSI) (U0901-52), SPI RECEIVE DATA (SPI MISO) (U0901-51), SPI CLK (SPI CLCK BUF) (U0901-53) and a control head select line (CNTL HD CE) (U0901-54). This BUS is a synchronous bus, in that the timing clock signal SPI CLCK is sent while SPI data (SPI TRANSMIT DATA or SPI RECEIVE DATA) is sent. Therefore, whenever there is activity on either SPI TRANSMIT DATA or SPI RECEIVE DATA there should be a uniform signal on SPI CLK. The SPI TRANSMIT DATA is used to send serial from the host radio to the control head μP, and SPI RECEIVE DATA is used to send data from the control head μP to the host radio.

When the host radio needs to communicate to the control head μP it brings the control head select line (CNTL HD CE) to a logic '0' and then sends the proper data and clock signals. After the data has been sent the control head select line is returned to a logic '1'. When the control head μP wants to communicate to the host radio the μP brings request line CNTL HD REQ to a logic '0' by switching on transistor Q0931 via μP pin 11. The host radio then starts communication by activating the control head select line (CNTL HD CE), sending the clock signal and sending data via SPI MOSI or receiving data via SPI MISO and buffer U0931-1.

## 3.7 Keypad Keys

The control head keypad is a 26 - key keypad. All keys are configured as 6 analogue lines (AN 0 - 5) to the control head μP. Lines AN 0 - 3 each control four keys, lines AN 4, 5 each control five keys. The voltage on the analogue lines varies between 0V and +5V depending on which key has been pressed. If a button is pressed, it will connect one of the 6 lines AN 0 - 5 to a resistive voltage divider R0807 - R0811 connected to +5V. The voltages of the lines are A/D converted inside the μP (ports PE 0 - 5) and specify the pressed button.

## 3.8 Status LED and Back Light Circuit

All the indicator LEDs (D0881 - D0884) are driven by current sources Q0881 - Q0883. To change the LED status the host radio sends a data message via SERIAL PERIPHERAL INTERFACE (SPI) to the control head μP. The control head μP determines the LED status from the received message and switches the LEDs on or off via pins 5, 6, 7. The LED status is stored in the μP's memory. The LED current is determined by the resistor at the emitter of the respective current source transistor.

The backlight for the LCD and the keypad is controlled by the host radio the same way as the indicator LEDs using μP pins 8, 9, 10. The keypad backlight current is drawn from the FLT A+ source and controlled by transistor Q0851. The current flowing through the LEDs cause a proportional voltage drop across the parallel resistors R0861, R0862. This voltage drop is amplified by the op-amp U0831-2. U0831-2 and Q0852 form a differential amplifier. The voltage difference between the base of Q0852 and the output of U0831-2 determines the current from the base of the LED control transistor Q0851 and in turn the brightness of the LEDs. The μP can switch the LEDs on and off by a logic high or low level at the port connected to the base of Q0852. If the base of Q0852 is at ground level, Q0852 is switched off and no current flows through Q0851 and the LEDs. If the μP port changes to +5V a current flows through Q0852 and in turn through Q0851 causing the LEDs to turn on and a rising voltage drop across R0861, R0862. The rising voltage causes the output of the op-amp to rise and to reduce the base to emitter voltage of Q0852. This decreases the current of Q0852 until the loop has settled. The backlight for the LCD uses a similar circuit. By using two μP ports (pin 8, 9) and different weighting resistors R0837 and R0838 the base of Q0832 can be set to four different voltage levels. This allows to switch the LEDs off or to select among three levels of brightness.

## 3.9 Liquid Crystal Display (LCD)

The LCD module U0902 consists of the display and the display driver. The display is a single layer super twist nematic (STN) LCD display. It has a dot matrix of 24 x120 dots for displaying graphics and alpha - numerical information, a line with 19 pre - defined icons below the dot matrix and line with 11 bars below the icon line. Six of the bars can be used to display the status of the keys located below.

The display driver is fixed on the flex which connects the display to the PC board. The driver contains a data interface to the µP, an LCD segment driver, an LCD power circuit, an oscillator, data RAM and control logic. At power up the driver's control logic is reset by a logic '0' at input RES (U0902-9). Resistor R0946 sets the driver's internal oscillator to about 18 kHz. By connecting U0902 pin 12 to +5V the driver's µP interface is configured to accept 8 bit parallel data input (U0902-D0-D7) from the control head µP (U0901 port PC0-PC7). Pin 15 connected to +5V sets the 6800 µP control mode.

To write data to the driver's RAM the µP sets chip select (U0902-14) to logic '1' via U0901-59 and R/W (U0902-17) to logic '0' via U0901-56. With input A0 (U0902-16) set to logic '0' via U0901-58 the µP writes control data to the driver. Clock signal E at pin 18 generated by µP pin 57, shifts 8 bit parallel data into the driver. Control data includes the RAM start address for the following display data. With input A0 set to logic '1' the µP then writes the display data to the display RAM. When data transfer is complete the µP terminates the chip select and the clock activities.

The voltage supply for the display is provided by the display driver power circuit. This circuit consists of a voltage multiplier, voltage regulator and a voltage follower. To use an external voltage supply the built-in power circuit can be turned off by a control command. The settings of the inputs T1 (U0902-36) and T2 (U0902-35) select among the various functions of the power circuit. With both inputs set to ground level by resistors R0955 and R0956 the voltage multiplier, the voltage regulator and the voltage follower are activated and no external voltage supply is required for the LCD. The external capacitors C0951 - C0953 configure the multiplier to triple the supply voltage. If R0957 is used instead of C0952 the multiplier doubles the supply voltage. In this configuration the multiplier output VOUT (U0902-42) supplies a voltage of -5V (2* -5V below VDD). The multiplied voltage VOUT is sent to the internal voltage regulator. To set the voltage level of the regulator output V5 (U0902-43) this voltage is divided by the resistors R0958 and R0959 and feed back to the reference input VR (U0902-44). In addition the regulator output voltage V5 can be controlled electronically by a control command sent to the driver. With the used configuration the voltage V5 is about -3V. The voltage V5 is resistively divided by the driver's voltage follower to provide the voltages V1 - V4. These voltages are needed for driving the liquid crystals. The driver circuit can be configured to use externally generated voltages for VOUT and V1 - V5. In this case the +5V supply voltage is multiplied by the µP (U0901-62) along with the multiplier circuit D0911, C0911, C0912, R0911 and R0913. The µP provides a square wave signal at pin 62 to drive the multiplier circuit. The voltages V1-V4 are generated from VOUT or V5 by the resistive divider R0941 - R0945 and supplied to the driver ports V1 - V5. Dependent on the configuration the level of VOUT or V5 can be measured by one of the µP's analogue to digital converters (U0901-20) via resistive divider R0914, R0915. To stabilize the display brightness over a large temperature range the µP measures the temperature via analogue to digital converter (U0901-18) using thermistor R0918 and resistor R0917. Dependent on the measured temperature the µP adjusts the driver output voltage V5, and in turn the display brightness, via parallel interface.

## 3.10 Microphone Connector

Signals BUS+, PTT, HOOK, MIC HI, HANDSET AUDIO and FLT A+ available at the microphone connector J0903, are connected to the radio's controller section via connector J0901.

## 3.11 Electrostatic Transient Protection

Electrostatic transient protection is provided for the sensitive components in the control head by diodes VR0901 - VR0905, VR0931 - VR0935. The diodes limit any transient voltages to tolerable levels. The associated capacitors provide Radio Frequency Interference (RFI) protection.

# Chapter 2.2

## PCB/Schematic Diagram and Parts List

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# Chapter 3

# UHF/VHF Radio - Level 3 Information

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# Chapter 3.1

## Introduction/Theory of Operation

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## VHF (136-174MHz) SPECIFIC CIRCUIT DESCRIPTION

# 1.0 Introduction

This section provides a detailed theory of operation for the radio and its components. The main radio is a single board design, consisting of the transmitter, receiver, and controller circuits.

The main board is designed to accept one additional option board. This may provide functions such as secure voice/data or DTMF decoder. The control head is mounted directly on the front of the radio or connected via an extension cable in remote mount operation. The control head contains LED indicators, a microphone connector, buttons/keypad and a display. These provide the user with interface control over the various features of the radio.

In addition to the power cable and antenna cable, an accessory cable can be attached to a connector on the rear of the radio. The accessory cable provides the necessary connections for items such as external speaker, emergency switch, foot operated PTT, ignition sensing, etc.

# 2.0 Open Controller

## 2.1 General

The radio controller consists of 4 main subsections:

- ☐ Digital Control
- ☐ Audio Processing
- ☐ Power Control
- ☐ Voltage Regulation

The digital control section of the radio board is based upon an open architecture controller configuration. It consists of a microprocessor, support memory, support logic, signal MUX ICs, the On/Off circuit, and general purpose Input/Output circuitry.

The controller uses the Motorola 68HC11K1 microprocessor (U0101). In addition to the microprocessor, the controller has 3 external memory devices. The 3 memory devices consist of a 32kbyte SRAM (U0103), a 512kbyte FLASH EEPROM (U0102), and a 16kbyte EEPROM (U0104).

**Note:** From this point on the 68HC11K1 microprocessor will be referred to as µP or K1µP. References to the control head will be to the Display/Keypad radio model (K6).

## 2.2 Voltage Regulators

Voltage regulation for the controller is provided by 3 separate devices; U0631 (LP2951CM) +5V, U0601 (LM2941T) +9.3V, and UNSW 5V (a combination of R0621 and VR0621). An additional regulator is located in the RF section.

Voltage regulation providing 5V for the digital circuitry is done by U0631. Input and output capacitors (C0631/C0632 and C0633-C0635) are used to reduce high frequency noise and provide proper operation during battery transients. This regulator provides a reset output (pin 5) that goes to 0 volts if the regulator output goes out of regulation. This is used to reset the controller to prevent improper operation. Diode D0631 prevents discharge of C0632 by negative spikes on the 9V3 voltage.

Regulator U0601 is used to generate the 9.3 volts required by some audio circuits, the RF circuitry and power control circuitry. Input and output capacitors (C0601-C0603 and C0604/C0605) are used to reduce high frequency noise. R0602/R0603 set the output voltage of the regulator. If the voltage at pin 1 is greater than 1.3 volts the regulator output decreases and if the voltage is less than 1.3 volts the regulator output increases. This regulator output is electronically enabled by a 0 volt signal on pin 2. Q0601 and associated circuitry (R0601/R0604/R0605) are used to disable the regulator when the radio is turned off.

UNSW 5V is only used in a few areas which draw low current and require 5 V while the radio is off.

UNSW 5V CL is used to buffer the internal RAM. C0622 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0621 prevents radio circuitry from discharging this capacitor.

The voltage 9V3 SUPP is only used in the VHF radio (T1) to supply the drain current for the RF MOS FET in the PA. The voltage SW B+ is monitored by the µP through the voltage divider R0641/R0642 and line BATTERY VOLTAGE. Diode VR0641 limits the divided voltage to 5.1V to protect the µP.

Diode D5601 (UHF) / D3601 (VHF) / D2601 (MB) located on the PA section acts as protection against transients and wrong polarity of the supply voltage.

## 2.3 Electronic On/Off

The radio has circuitry which allows radio software and/or external triggers to turn the radio on or off without direct user action. For example, automatic turn on when ignition is sensed and off when ignition is off.

Q0611 is used to provide SW B+ to the various radio circuits. Q0611 contains a pnp and an npn transistor and acts as an electronic on/off switch. The switch is on when the collector of the npn transistor (Q0611-1) is low. When the radio is off the pnp transistor is cutoff and the voltage at pin 1 is at A+. This effectively prevents current flow through the pnp transistor from emitter (pin 3) to collector (pin 2).

When the radio is turned on the voltage at the Q0611 pin 4 is high (about 4.4V) and the npn transistor switches on (saturation) and pulls down the voltage at the base of the pnp transistor. With Transistor Q0611 now “enabled” current flows through the device from pin 3 to pin 2. This path has a very low impedance (less than 1 ohm) from emitter to collector. This effectively provides the same voltage level at SWB+ as at A+.

The electronic on/off circuitry can be enabled by the microprocessor (through ASFIC port GCB2, line B+ CONTROL), the emergency switch (line EMERGENCY CONTROL), the mechanical On/Off button on the control head (line ON OFF CONTROL), or the ignition sense circuitry (line IGNITION CONTROL). If any of the 4 paths cause a low at Q0611 pin 1, the electronic ON is engaged.

## 2.4 Emergency

The emergency switch (J0400-9), when engaged, grounds the base of Q0441 and pulls the line EMERGENCY CONTROL to low via D0441. EMER IGN SENSE is pulled high by R0441. When the emergency switch is released the base of Q0441 is pulled high by R0442. This causes the collector of transistor Q0441 to go low (0.2V), thereby setting the EMER IGN SENSE line to low.

While EMERGENCY CONTROL is low, SW B+ is on, the microprocessor starts execution, reads that the emergency input is active through the voltage level of EMER IGN SENSE, and sets the B+ CONTROL output of the ASFIC pin B4 to a logic high. This high will keep Q0611 switched on. This operation allows a momentary press of the emergency switch to power up the radio. When the microprocessor has finished processing the emergency press, it sets the B+ CONTROL line to a logic 0. This turns off Q0611 and the radio turns off. Notice that the microprocessor is alerted to the emergency condition via line EMER IGN SENSE. If the radio was already on when emergency was triggered then B+ CONTROL would already be high.

## 2.5 Mechanical On/Off

This refers to the typical on/off button, located on the control head, and which turns the radio on and off. If the radio is turned off and the on/off button is pressed, line ON OFF CONTROL goes high and switches the radio on as long as the button is pressed. The microprocessor is alerted through line ANALOG 3 which is pulled to low by Q0925 (Display/Keypad Control Head) while the on/off button is pressed. If the software detects a low state it asserts B+ CONTROL via ASFIC pin B4 high which keeps Q0611, and in turn the radio switched on.

If the on/off button is pressed and held while the radio is on, the software detects the line ANALOG 3 changing to low and switches the radio off by setting B+ CONTROL to low.

## 2.6 Ignition

Ignition sense is used to prevent the radio from draining the vehicle's battery because the engine is not running.

When the IGNITION input (J0400-10) goes above 6 volts Q0611 is turned on via line IGNITION CONTROL. Q0611 turns on SW B+ and the microprocessor starts execution. A high IGNITION input reduces the voltage of line EMER IGN SENSE by turning on Q0450. The software reads the line EMER IGN SENSE, determines from the level (Emergency has a different level) that the IGNITION input is active and sets the B+ CONTROL output of the ASFIC pin B4 to high to latch on SW B+.

When the IGNITION input goes below 6 volts, Q0450 switches off and R0449, R0450 pull line EMER IGN SENSE high. The software is alerted by line EMER IGN SENSE to switch off the radio by setting B+ CONTROL to low. The next time the IGNITION input goes above 6 volts the above process will be repeated.

## 2.7 Hook RSS

The HOOK RSS input is used to inform the µP when the Microphone's hang-up switch is engaged. Dependent on the radio model the µP may take actions like turning the audio PA on or off.
The signal is routed from J0101-3 and J0400-14 through transistor Q0101 to the K1µP U0101-23. The voltage range of HOOK RSS in normal operating mode is 0-5V.

To start SBEP communication this voltage must be above 6V. This condition generates a µP interrupt via VR0102, Q0105, Q0104, Q0106 and enables the BUS+ line for communication via Q0122, Q0121.

## 2.8 Microprocessor Clock Synthesizer

The clock source for the microprocessor system is generated by the ASFIC (U0201). Upon power-up the synthesizer U5701 (UHF) / U3701 (VHF) / U2701 (MB) generates a 2.1 MHz waveform that is routed from the RF section (via C0202) to the ASFIC (on U0201-E1) For the main board controller the ASFIC uses 2.1MHz as a reference input clock signal for its internal synthesizer. The ASFIC, in addition to audio circuitry, has a programmable synthesizer which can generate a synthesized signal ranging from 1200Hz to 32.769MHz in 1200 Hz steps.

When power is first applied, the ASFIC will generate its default 3.6864 MHz CMOS square wave μP CLK (on U0201-D1) and this is routed to the microprocessor (U0101-73). After the microprocessor starts operation, it reprograms the ASFIC clock synthesizer to a higher μP CLK frequency (usually 7.9488 MHz) and continues operation.

The ASFIC may be reprogrammed to change the clock synthesizer frequencies at various times depending on the software features that are executing. In addition, the clock frequency of the synthesizer is changed in small amounts if there is a possibility of harmonics of this clock source interfering with the desired radio receive frequency.

The ASFIC synthesizer loop uses C0228, C0229 and R0222 to set the switching time and jitter of the clock output. If the synthesizer cannot generate the required clock frequency it will switch back to its default 3.6864MHz output.

Because the ASFIC synthesizer and the μP system will not operate without the 2.1MHz reference clock, it (and the voltage regulators) should be checked first when debugging the system.

## 2.9 Serial Peripheral Interface (SPI)

The μP communicates to many of the ICs through its SPI port. This port consists of SPI TRANSMIT DATA (MOSI) (U0101-1), SPI RECEIVE DATA (MISO) (U0101-80), SPI CLK (U0101-2) and chip select lines going to the various ICs, connected on the SPI PORT (BUS). This BUS is a synchronous bus, in that the timing clock signal CLK is sent while SPI data (SPI TRANSMIT DATA or SPI RECEIVE DATA) is sent. Therefore, whenever there is activity on either SPI TRANSMIT DATA or SPI RECEIVE DATA there should be a uniform signal on CLK. The SPI TRANSMIT DATA is used to send serial from a μP to a device, and SPI RECEIVE DATA is used to send data from a device to a μP. The only device from which data can be received via SPI RECEIVE DATA is the EEPROM (U0104 or U0107) and a control head with graphical display (Display/Keypad Radio Model K6).

On the controller there are three ICs on the SPI BUS, ASFIC (U0201-F2), EEPROM (U0104-1 or U0107-1) and D/A (U0731-6). In the RF sections there is one IC on the SPI BUS which is the FRAC-N Synthesizer. The SPI TRANSMIT DATA and CLK lines going to the RF section are filtered by L0131/L0132 to minimize noise. The chip select lines for the IC´s are decoded by the address decoder U0105.

The SPI BUS is also used for the control head. U0106-2,3 buffer the SPI TRANSMIT DATA and CLK lines to the control head. U0106-1 switch off the CLK signal for the LCD display if it is not selected via LCD CE and Q0141.

When the μP needs to program any of these IC's it brings the chip select line for that IC to a logic 0 and then sends the proper data and clock signals. The amount of data sent to the various IC's are different, for example the FRAC-N can receive up to 21 bytes (168 bits) while the DAC can receive up to 3 bytes (24 bits). After the data has been sent the chip select line is returned to a logic 1.

When the control head with graphical display wants to communicate to the µP it brings request line ANALOG 2 (J0101-11) to a logic “0“. The µP reads this line via one of the analogue to digital converters (U0101-48) and then starts communication by activating the control head select line (LED CHT CE) via U0105-9 and J0101-12, sending the clock signal via U0106-3 and J0101-5 and sending data via U0106-2 and J0101-6 or receiving data via J0101-10 and gate U0171. During data transfer gate U0171 is switched on by line LED CHT CE via transistor Q0171 and gate U0172-1. Gate U0172-1 is enabled by the µP via ASFIC output GCB4 (U0201-A2).

The Option board interfaces are different in that the µP can also read data back from devices connected.The timing and operation of this interface is specific to the option connected, but generally follows the pattern:

1. an option board device generates an interrupt via J0103-8, Q0124, Q0125 and µP pin 61 (IRQ). The µP determines the interrupt source by reading a high at the collector of Q0124 via µP pin 7 and R0129.
2. the main board asserts a chip select for that option board device via U0105-10, J0102-5,
3. the main board µP generates the CLK (J0102-6),
4. the main board µP writes serial data via J0102-4 and reads serial data via J0102-2 and,
5. when data transfer is complete the main board terminates the chip select and CLK activity.

## 2.10 SPEB Serial Interface

The SBEP serial interface allows the radio to communicate with the Dealer Programming Software (DPS) via the Radio Interface Box (RIB). This interface connects to the Microphone connector (J0903/J0803) via Control Head connector (J0101-15) or to the accessory connector J0400-6 and comprises BUS+ (J0101-15). The line is bi-directional, meaning that either the radio or the DPS can drive the line.

When the RIB (Radio Interface Box) is connected to the radio, a voltage on the HOOK RSS line above 6 volts switches on Q0105. The low state at collector of Q0105 switches Q0104 off and in turn, Q0106 on. A high to low transition at the collector of Q0106 generates an interrupt via µP pin 61. The µP determines the interrupt source by reading a high at the collector of Q0104 via µP pin 6 and R0125. The switched on Q0105 also switches off Q0122 enabling the µP to read BUS+ via pin 78 and to write BUS+ via pin 79 and transistors Q0123, Q0121. While the radio is sending serial data at pin 79 via Q0123 and Q0121 it receives an “echo” of the same data at pin 78.

When the voltage on the HOOK RSS line is below 6 volts (RIB is not connected), the high collector of Q0105 turns on Q0122. The low collector of Q0122 prevents the µP from writing data to BUS+ via Q0123. In this mode line BUS+ is used for signal SCI RX of the Serial Communication Interface (SCI). The µP reads the SCI via signal SCI RX (pin 78) and writes via signal SCI TX (pin 79). Both signals are available on the accessory connector J0400 (SCI DATA OUT, SCI DATA IN).

## 2.11 General Purpose Input/Output

The Controller provides one general purpose line (GP I/O) available on the accessory connector J0400-12 to interface to external options. The software and the hardware configuration of the radio model defines the function of the port. The port uses an output transistor (Q0432) controlled by μP via ASFIC port GCB3 (pin B3).

An external alarm output, available on J0400 pin 4 is generated by the μP via ASFIC port GCB1 (pin A3) and transistor Q0411. Input EXTERNAL PTT on J0400 pin 3 is read by the μP via line REAR PTT and μP pin 8.

Pin 13 of the accessory connector J0400 provides a voltage at battery level while the radio is switched on. The output is capable to drive a dc current up to 20mA. When the radio is switched on, the voltage 9V3 turns on transistor Q0482. Transistor Q0482 switches on Q0481 and enables a current flow from emitter to collector of Q0481. This path has a very low impedance and effectively provides the same voltage level at SW FLT A+ as at FLT A+. If the radio is switched off the voltage 9V3 is at ground level which switches off Q0482 and in turn cuts off the current from emitter to collector of Q0481.

## 2.12 Normal Microprocessor Operation

For this radio, the μP is configured to operate in one of two modes, expanded and bootstrap. In expanded mode the μP uses external memory devices to operate, whereas in bootstrap operation the μP uses only its internal memory. In normal operation of the radio the μP is operating in expanded mode as described below.

In expanded mode on this radio, the μP (U0101) has access to three external memory devices; U0102 (FLASH EEPROM), U0103 (SRAM), U0104 or U0107 (optional EEPROM). Also, within the μP there are 768 bytes of internal RAM and 640 bytes of internal EEPROM, as well as logic to select external memory devices.

The (optional) external EEPROM (U0104 or U0107) as well as the μP's own internal EEPROM space contain the information in the radio which is customer specific, referred to as the codeplug. This information consists of items such as: 1) what band the radio operates in, 2) what frequencies are assigned to what channel, and 3) tuning information. In general tuning information and other more frequently accessed items are stored in the internal EEPROM (space within the 68HC11K1), while the remaining data is stored in the external EEPROM. (See the particular device subsection for more details.)

The external SRAM (U0103) as well as the μP's own internal RAM space are used for temporary calculations required by the software during execution. All of the data stored in both of these locations is lost when the radio powers off (See the particular device subsection for more details).

The FLASH EEPROM contains the actual Radio Operating Software. This software is common to all open architecture radios within a given model type. For example Securenet radios may have a different version of software in the FLASH EEPROM than a non-secure radio (See the particular device subsection for more details).

The K1μP provides an address bus of 16 address lines (A0-A15), and a data bus of 8 data lines (D0-D7). There are also three control lines; CSPROG (U0101-29) to chip select U0102-30 (FLASH EEPROM), CSGP2 (U0101-28) to chip select U0103-20 (SRAM) and PG7_R_W to select whether to read or to write. All other chips (ASFIC/PENDULLUM/DAC/FRACN/LCD/LED/optional EEPROM/ OPTION BOARD) are selected by 3 lines of the μP using address decoder U0105. When the μP is functioning normally, the address and data lines should be toggling at CMOS logic levels.

Specifically, the logic high levels should be between 4.8 and 5.0 V, and the logic low levels should be between 0 and 0.2 V. No other intermediate levels should be observed, and the rise and fall times should be <30 ns.

The low-order address lines (A0-A7) and the data lines (D0-D7) should be toggling at a high rate, i.e., you should set your oscilloscope sweep to 1 us/div. or faster to observe individual pulses. High speed CMOS transitions should also be observed on the µP control lines.

On the µP the lines XIRQ (U0101-30), MODA LIR (U0101-77), MODB VSTPY (U0101-76) and RESET (U0101-75) should be high at all times during normal operation. Whenever a data or address line becomes open or shorted to an adjacent line, a common symptom is that the RESET line goes low periodically, with the period being in the order of 20 msecs. In the case of shorted lines you may also detect the line periodically at an intermediate level, i.e. around 2.5 V when 2 shorted lines attempt to drive to opposite rails.

The MODA LIR (U0101-77) and MODB VSTPY (U0101-76) inputs to the µP must be at a logic 1 for it to start executing correctly. After the µP starts execution it will periodically pulse these lines to determine the desired operating mode. While the Central Processing Unit (CPU) is running, MODA LIR is an open-drain CMOS output which goes low whenever the µP begins a new instruction (an instruction typically requires 2-4 external bus cycles, or memory fetches).

However, since it is an open-drain output, the waveform rise assumes an exponential shape similar to an RC circuit.

There are eight analogue to digital converter ports (A/D) on U0101. They are labelled within the device block as PE0-PE7. These lines sense the voltage level ranging from 0 to 5 V of the input line and convert that level to a number ranging from 0 to 255 which can be read by the software to take appropriate action.

For example, U0101-46 is the battery voltage detect line. R0641 and R0642 form a resistor divider on SWB+. With 30K and 10K and a voltage range of 11 V to 17 V, that A/D port would see 2.74 V to 4.24 V which would then be converted to ~140 to 217 respectively.

U0101-51 is the high reference voltage for the A/D ports on the µP. Resistor R0106 and capacitor C0106 filter the +5 V reference. If this voltage is lower than +5 V the A/D readings will be incorrect. Likewise U0101-50 is the low reference for the A/D ports. This line is normally tied to ground. If this line is not connected to ground, the A/D readings will be incorrect.

Capacitors C0104, C0105, C0113, C0114 serve to filter out any AC noise which may ride on +5V at U0101.

Input IRQ (U101-61) generates an interrupt, if either HOOK RSS (J0101-3) is higher than 6V (SBEP communication) and turns Q0106 on via Q0105, Q0104, or a low at the option interrupt pin (J0103-8) turns Q0124 off and Q0125 on. The µP determines the interrupt source by reading the collector of Q0104 via U0101-6 and the collector Q0124 via U0101-7.

## 2.13 FLASH Electronically Erasable Programmable Memory (FLASH EEPROM)

The 512 KByte FLASH EEPROM (U0102) contains the radio operating software. This software is common to all open architecture radios within a given model type. This is, as opposed to the codeplug information stored in EEPROM (U0104) which could be different from one user to another in the same company.

In normal operating mode, this memory is only read, not written to. The memory access signals (CE, OE and WE) are generated by the μP.

To upgrade/reprogram the FLASH software, the μP must be set in bootstrap operating mode, and the FLASH device pin (U0102-9) $V_{pp}$ must be between 11.4 and 12.6 V. This voltage switches Q0102 on and in turn Q0103 off. The low state at collector of Q0102 pulls MODA LIR (U0101-77) and MODB VSTBY (U0101-76) via diode D0101 to low which enables the bootstrap operating mode after power up. The high state at collector of Q0103 enables the μP to control the FLASH EN OE (U0102-32) input via U0106-4. Chip select (U102-30) and read or write operation (U102-7) are controlled by μP pins 29 and 33. In normal operating mode $V_{PP}$ is below 5V which switches Q0102 off and Q0103 on.

The FLASH device may be reprogrammed 1,000 times without issue. It is not recommended to reprogram the FLASH device at a temperature below 0°C.

Capacitor C0131 serves to filter out any AC noise which may ride on +5V at U0101, and C0132 filters out any AC noise on $V_{pp}$.

## 2.14 Electrically Erasable Programmable Memory (EEPROM)

The optional EEPROM (U0104 or U0107) contains additional radio operating parameters such as operating frequency and signalling features, commonly known as the codeplug. It is also used to store radio operating state parameters such as current mode and volume. U0104 can have up to 8kbyte and U0107 up to 16 kbyte. This memory can be written to in excess of 100,000 times and will retain the data when power is removed from the radio. The memory access signals (SI, SO and SCK) are generated by the μP and chip select (CS) is generated by address decoder U0105-4.

Additional EEPROM is contained in the μP (U0101). This EEPROM is used to store radio tuning and alignment data. Like the external EEPROM this memory can be programmed multiple times and will retain the data when power is removed from the radio.

**Note:** The external EEPROM plus the 640 bytes of internal EEPROM in the 68HC11K1 comprise the complete codeplug.

## 2.15 Static Random Access Memory (SRAM)

The SRAM (U0103) contains temporary radio calculations or parameters that can change very frequently, and which are generated and stored by the software during its normal operation. The information is lost when the radio is turned off. The device allows an unlimited number of write cycles. SRAM accesses are indicated by the CS signal U103-20 (which comes from U101-CSGP2) going low. U0103 is commonly referred to as the external RAM as opposed to the internal RAM which is the 768 bytes of RAM which is part of the 68HC11K1. Both RAM spaces serve the purpose. However, the internal RAM is used for the calculated values which are accessed most often. Capacitor C0133 serves to filter out any ac noise which may ride on +5V at U0103.

# CONTROLLER BOARD AUDIO AND SIGNALLING CIRCUITS

# 3.0 General

## 3.1 Audio Signalling Filter IC (ASFIC)

The ASFIC (U0201) used in the controller has 4 functions;

- ☐ RX/TX audio shaping, i.e. filtering, amplification, attenuation
- ☐ RX/TX signalling, PL/DPL/HST/MDC/MPT
- ❑ Squelch detection
- ❑ Microprocessor clock signal generation (see Microprocessor Clock Synthesizer Description Block).

The ASFIC is programmable through the SPI BUS (U0201-E3/F1/F2), normally receiving 21 bytes. This programming sets up various paths within the ASFIC to route audio and/or signalling signals through the appropriate filtering, gain and attenuator blocks. The ASFIC also has 6 General Control Bits GCB0-5 which are CMOS level outputs and used for AUDIO PA ENABLE (GCB0) to switch the audio PA on and off, EXTERNAL ALARM (GCB1) and B+ CONTROL (GCB2) to switch the voltage regulators (and the radio) on and off. GCB3 controls output GPI/O (accessory connector J0400-12), HIGH LOW BAND (GCB4) can be used to switch between band splits and GCB5 is available on the option board connector J0102-3. Output GCB4 controls gate U0171 via U0172-1 which enables the µP to receive data from the control head. The supply voltage for the ASFIC has additional filtering provided by Q0200, D0200, R0200, L0200 and C0200. Diode D0200 increases the voltage at the base of Q0200 about 0.6 volts above the 5 volt supply voltage to compensate the base - emiter voltage drop of Q0200.

## 3.2 Audio Ground

VAG is the dc bias used as an audio ground for the op-amps that are external to the Audio Signalling Filter IC (ASFIC). U0251-1 form this bias by dividing 9.3V with resistors R0251, R0252 and buffering the 4.65V result with a voltage follower. VAG emerges at pin 1 of U0251-1. C0253 is a bypass capacitor for VAG. The ASFIC generates its own 2.5V bias for its internal circuitry. C0221 is the bypass for the ASFIC's audio ground dc bias. Note that while there are ASFIC VAG, and BOARD VAG (U0201-1) each of these are separate; they do not connect together.

# 4.0 Transmit Audio Circuits

Refer to Figure 3-1 for reference for the following sections.

## 4.1 Mic Input Path

The radio supports two distinct microphone paths known as internal (from Control Head) and external mic (from accessory connector J0400-2) and an auxiliary path (FLAT TX AUDIO). The microphones used for the radio require a DC biasing voltage provided by a resistive network.

These two microphone audio inputs are connected together through R0413; resistors R0414 and R0415 are not placed. Following the internal mic path; the microphone is plugged into the radio control head and is connected to the controller board via J101-16.

From here the signal is routed to R0206. R0204 and R0205 provide the 9.3VDC bias and R0206 provides input protection for the CMOS amplifier input. R0205 and C0209 provide a 1kΩ AC path to ground that sets the input impedance for the microphone and determines the gain based on the emitter resistor in the microphone's amplifier circuit.

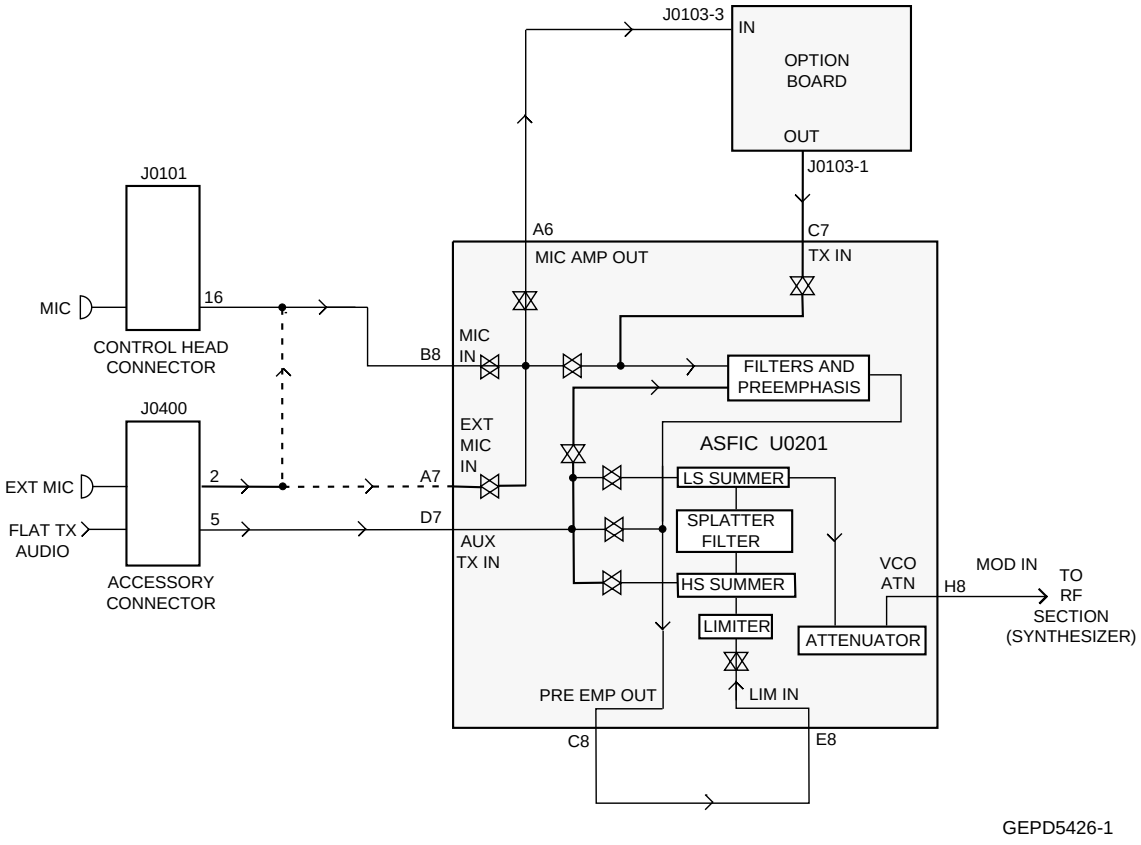


**Figure 3-1** Transmit Audio Paths

Filter capacitor C0210 provides low-pass filtering to eliminate frequency components above 3 kHz, and C0211 serves as a DC blocking capacitor. The audio signal at U0201-B8 should be approximately 80mV for 1.5kHz or 3kHz of deviation with 12.5kHz or 25 kHz channel spacing. The FLAT TX AUDIO signal from accessory connector J0400-5 is buffered by op-amp U0202-1 and fed to the ASFIC U0201-D7 through C0205.

## 4.2 External Mic Path

The external microphone signal enters the radio on accessory connector J0400 pin 2 and connects to the standard microphone input through R0413. Components R0414 - R0416, C0413, C0414, C0417 are not used.

## 4.3 PTT Sensing and TX Audio Processing

Mic PTT coming from the Control Head via connector J101-4 is sensed by the µP U0101 pin 22. An external PTT can be generated by grounding pin 3 on the accessory connector. When microphone PTT or externalPTT is sensed, the µP will always configure the ASFIC for the ”internal” mic audio path.

Inside the ASFIC, the MIC audio is filtered to eliminate frequency components outside the 300-3000Hz voice band, pre-emphasized if pre-emphasis is enabled. The capacitor between ASFIC pre-emphasis out U0201-C8 and ASFIC limiter in U0201-E8 AC couples the signal between ASFIC blocks and prevents the DC bias at the ASFIC output U0201-H8 from shifting when the ASFIC transmit circuits are powered up. The signal is then limited to prevent the transmitter from over deviating. The limited MIC audio is then routed through a summer which, is used to add in signalling data, and then to a splatter filter to eliminate high frequency spectral components that could be generated by the limiter. The audio is then routed to two attenuators, which are tuned in the factory or the field to set the proper amount of FM deviation. The TX audio emerges from the ASFIC at U0201-H8 MOD IN, at which point it is routed to the RF section.

## 4.4 TX Secure Audio (optional)

The audio follows the normal transmit audio processing until it emerges from the ASFIC MIC AMP OUT pin (U0201-A6), which is fed to the Secure board residing at option connector J0103-3. The Secure board contains circuitry to amplify, encrypt, and filter the audio. The encrypted signal is then fed back from J0103-1 to the ASFIC TX IN input (U0201-C7). The signal level at this pin should be about 80mVrms. The signal is then routed through the TX path in the ASFIC and emerges at VCO ATN pin H8.

# 5.0 Transmit Signalling Circuits

Refer to Figure 3-2 for reference for the following sections. From a hardware point of view, there are three types of signalling:

1. Sub-audible data (PL/DPL/Connect Tone) that gets summed with transmit voice or signalling,
2. DTMF data for telephone communication in trunked and conventional systems, and
3. Audible signalling including Select 5, MPT-1327, MDC, High speed Trunking.

**NOTE:** All three types are supported by the hardware while the radio software determines which signalling type is available.

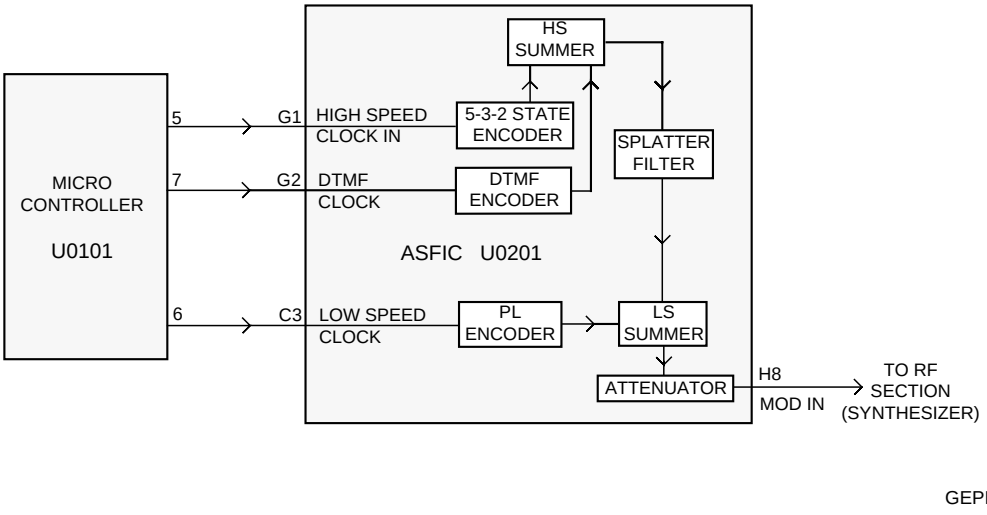


**Figure 3-2** Transmit Signalling Paths

## 5.1 Sub-audible Data (PL/DPL)

Sub-audible data implies signalling whose bandwidth is below 300Hz. PL and DPL waveforms are used for conventional operation and connect tones for trunked voice channel operation. The trunking connect tone is simply a PL tone at a higher deviation level than PL in a conventional system. Although it is referred to as ”sub-audible data,” the actual frequency spectrum of these waveforms may be as high as 250 Hz, which is audible to the human ear. However, the radio receiver filters out any audio below 300Hz, so these tones are never heard in the actual system.

Only one type of sub-audible data can be generated by U0201 (ASFIC) at any one time. The process is as follows, using the SPI BUS, the µP programs the ASFIC to set up the proper low-speed data deviation and select the PL or DPL filters. The µP then generates a square wave which strobes the ASFIC PL / DPL encode input PL CLK U0201-C3 at twelve times the desired data rate. For example, for a PL frequency of 103Hz, the frequency of the square wave would be 1236Hz.

This drives a tone generator inside U0201 which generates a staircase approximation to a PL sine wave or DPL data pattern. This internal waveform is then low-pass filtered and summed with voice or data. The resulting summed waveform then appears on U0201-H8 (MOD IN), where it is sent to the RF board as previously described for transmit audio. A trunking connect tone would be generated in the same manner as a PL tone.

## 5.2 High Speed Data

High speed data refers to the 3600 baud data waveforms, known as Inbound Signalling Words (ISWs) used in a trunking system for high speed communication between the central controller and the radio. To generate an ISW, the μP first programs the ASFIC (U0201) to the proper filter and gain settings. It then begins strobing U0201-G1 (TRK CLK IN) with a pulse when the data is supposed to change states. U0201's 5-3-2 State Encoder (which is in a 2-state mode) is then fed to the post-limiter summer block and then the splatter filter.

From that point it is routed through the modulation attenuators and then out of the ASFIC to the RF board. MPT 1327 and MDC are generated in much the same way as Trunking ISW. However, in some cases these signals may also pass through a data pre-emphasis block in the ASFIC. Also these signalling schemes are based on sending a combination of 1200 Hz and 1800 Hz tones only. Microphone audio is muted during High Speed Data signalling.

## 5.3 Dual Tone Multiple Frequency (DTMF) Data

DTMF data is a dual tone waveform used during phone interconnect operation. It is the same type of tones which are heard when using a "Touch Tone" telephone.

There are seven frequencies, with four in the low group (697, 770, 852, 941Hz) and three in the high group (1209, 1336, 1477Hz).

The high-group tone is generated by the μP (U0101-5) strobing U0201-G1 at six times the tone frequency for tones less than 1440Hz or twice the frequency for tones greater than 1440Hz. The low group tone is generated by the μP (U0101-7) strobing U0201-G2 (DTMF CLCK) at six times the tone frequency. Inside U0201 the low-group and high-group tones are summed (with the amplitude of the high group tone being approximately 2 dB greater than that of the low group tone) and then pre-emphasized before being routed to the summer and splatter filter. The DTMF waveform then follows the same path as was described for high-speed data.

# 6.0 Receive Audio Circuits

Refer to Figure 3-3 for reference for the following sections.

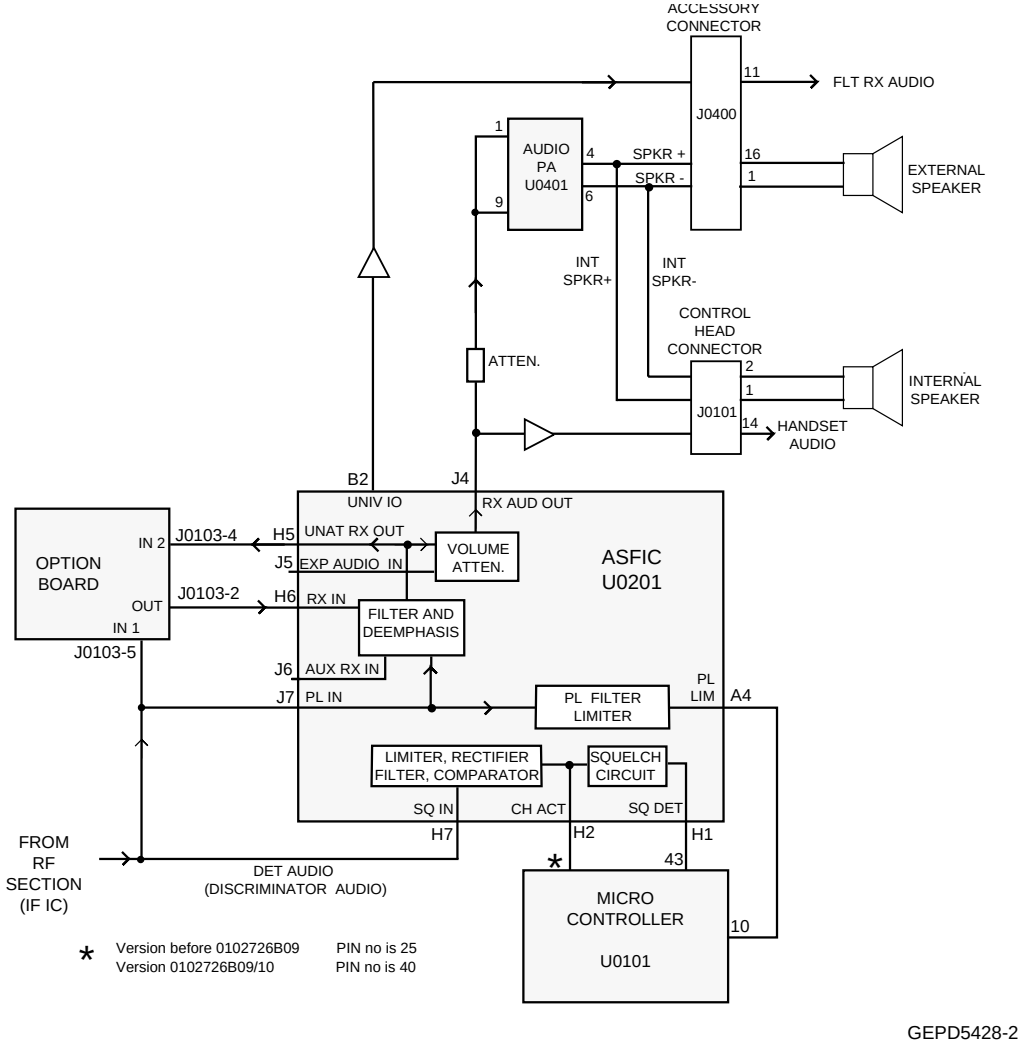


**Figure 3-3** Receive Audio Paths.

## 6.1 Squelch Detect

The radio's RF circuits are constantly producing an output at the discriminator U5201-28 (UHF) / U5201-28 (VHF) / U2201-28 (MB). This signal (DET AUDIO) is routed to the ASFIC's squelch detect circuitry input SQ IN (U0201-H7). All of the squelch detect circuitry is contained within the ASFIC. Therefore from a user's point of view, DET AUDIO enters the ASFIC, and the ASFIC produces two CMOS logic outputs based on the result. They are CH ACT (U0201-H2) and SQ DET (U0201-H1).

The squelch signal entering the ASFIC is amplified, filtered, attenuated, and rectified. It is then sent to a comparator to produce an active high signal on CH ACT. A squelch tail circuit is used to produce SQ DET (U0201-H1) from CH ACT. The state of CH ACT and SQ DET is high (logic 1) when carrier is detected, otherwise low (logic 0).

CH ACT is routed to the µP pin 40 while SQ DET adds up with LOCK DET, weighted by resistors R0113, R0114, and is routed to one of the µP´s ADC inputs U0101-43. From the voltage weighted by the resistors the µP determines whether SQ DET, LOCK DET or both are active.

SQ DET is used to determine all audio mute/unmute decisions except for Conventional Scan. In this case CH ACT is a pre-indicator as it occurs slightly faster than SQ DET.

## 6.2 Audio Processing and Digital Volume Control

The receiver audio signal enters the controller section from the IF IC U5201-28 (UHF) / U5201-28 (VHF) / U2201-28 (MB) on DET AUDIO and passes through RC filter, R0203 and C0208 which filters out IF noise. The signal is AC coupled by C0207 and enters the ASFIC via the PL IN pin U0201-J7.

Inside the ASFIC, the signal goes through 2 paths in parallel, the audio path and the PL/DPL path.

The audio path has a programmable amplifier, whose setting is based on the channel bandwidth being received, then a LPF filter to remove any frequency components above 3000Hz and then an HPF to strip off any sub-audible data below 300Hz. Next, the recovered audio passes through a de-emphasis filter if it is enabled (to compensate for Pre-emphasis which is used to reduce the effects of FM noise). The IC then passes the audio through the 8-bit programmable attenuator whose level is set depending on the value of the volume control. Finally the filtered audio signal passes through an output buffer within the ASFIC. The audio signal exits the ASFIC at RX AUDIO (U0201-J4).

The µP programs the attenuator, using the SPI BUS, based on the volume setting. The minimum / maximum settings of the attenuator are set by codeplug parameters.

Since sub-audible signalling is summed with voice information on transmit, it must be separated from the voice information before processing. Any sub-audible signalling enters the ASFIC from the IF IC at PL IN U0201-J7. Once inside it goes through the PL/DPL path.

The signal first passes through one of 2 low pass filters, either PL low pass filter or DPL/LST low pass filter. Either signal is then filtered and goes through a limiter and exits the ASFIC at PL LIM (U0201-A4). At this point the signal will appear as a square wave version of the sub-audible signal which the radio received. The microprocessor (U0101-10) will decode the signal directly to determine if it is the tone/code which is currently active on that mode.

## 6.3 Audio Amplification Speaker (+) Speaker (-)

The output of the ASFIC's digital volume pot, U0201-J4 is routed through a voltage divider formed by R0401 and R0402 to set the correct input level to the audio PA (U0401). This is necessary because the gain of the audio PA is 46 dB, and the ASFIC output is capable of overdriving the PA unless the maximum volume is limited.

The audio then passes through C0401 which provides AC coupling and low frequency roll-off. C0402 provides high frequency roll-off as the audio signal is routed to pins 1 and 9 of the audio power amplifier U0401.

The audio power amplifier has one inverted and one non-inverted output that produces the differential audio output SPK+ / SPK- (U0401-4/6). The inputs for each of these amplifiers are pins 1 and 9 respectively; these inputs are both tied to the received audio. The audio PA's DC biases are not activated until the audio PA is enabled at pin 8.

The audio PA is enabled via AUDIO PA ENABLE signal from the ASFIC (U0201-B5). When the base of Q0401 is low, the transistor is off and U0401-8 is high, using pull up resistor R0406, and the Audio PA is ON. The voltage at U0401-8 must be above 8.5VDC to properly enable the device. If the voltage is between 3.3 and 6.4V, the device will be active but has its input (U0401-1/9) off. This is a mute condition which is not employed in this radio design. R0404 ensures that the base of Q0401 is high on power up. Otherwise there may be an audio pop due to R0406 pulling U0401-8 high before the software can switch on Q0401.

The SPK+ and SPK- outputs of the audio PA have a DC bias which varies proportionately with FLT A+ (U0401-7). FLT A+ of 11V yields a DC offset of 5V, and FLT A+ of 17V yields a DC offset of 8.5V. If either of these lines is shorted to ground, it is possible that the audio PA will be damaged. SPK+ and SPK- are routed to the accessory connector (J400-16 and 1) and to the control head (connector J0101-1 and 2).

## 6.4 Handset Audio

Certain hand held accessories have a speaker within them which require a different voltage level than that provided by U0401. For those devices HANDSET AUDIO is available at J0101-14.

The received audio from the output of the ASFIC's digital volume attenuator is also routed to U0202-4 pin 9 where it is amplified 15 dB; this is set by the 10k/68k combination of R0233 and R0232. This signal is routed from the output of the op amp U202-4 pin 8 to J0101-14. The control head sends this signal directly out to the microphone jack. The maximum value of this output is 6.6Vp-p.

## 6.5 Filtered Audio

The ASFIC has an audio whose output at U0201-B2 has been filtered and de-emphasized, but has not gone through the digital volume attenuator. From ASFIC U0201-B2 the signal is AC coupled to U0202-2 by capacitor C0230. R0224 and R0225 determine the gain of op-amp U0202-2. The output of U0202-2 is the routed to J0400-11.Note that any volume adjustment of the signal on this path must be done by the accessory.

## 6.6 RX Secure Audio (optional)

Discriminator audio, which is now encrypted audio, enters the Secure board at connector J0103-5. On the Secure board, the encrypted signal is converted back to normal audio format, and then fed back through (J0103-2) to RX IN of the ASFIC (U0201-H6). From then on it follows a path identical to conventional receive audio, where it is filtered (0.3 - 3kHz) and de-emphasized. The signal UNAT RX OUT from the ASFIC (U0201-H5), also routed to option connector J0103-4, is not used for the Secure board but for other option boards.

# 7.0 Receive Signalling Circuits

Refer to Figure 3-4 for reference for the following sections.

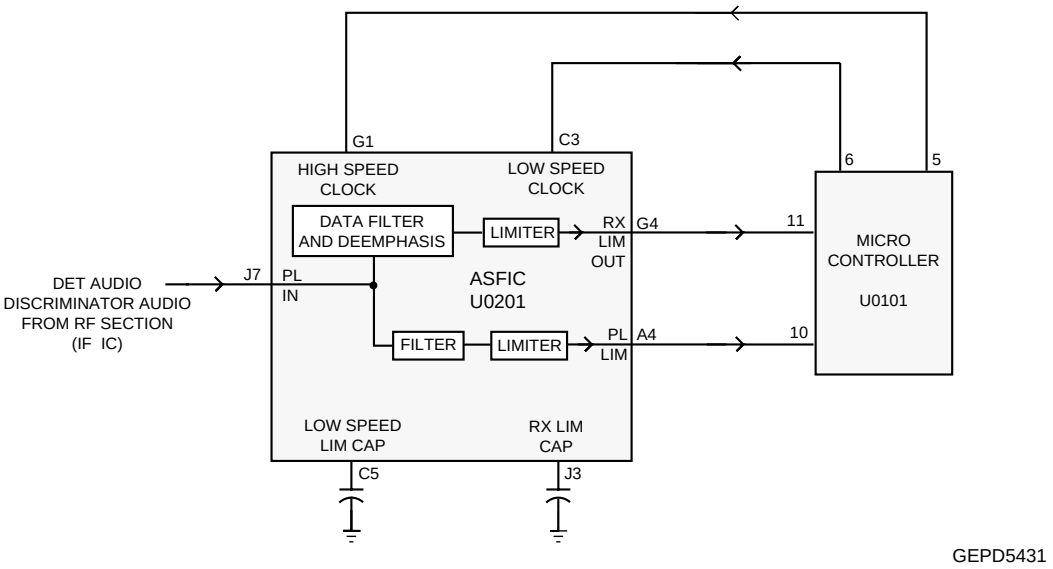


**Figure 3-4** Receive Signalling Path.

## 7.1 Sub-audible Data (PL/DPL) and High Speed Data Decoder

The ASFIC (U0201) is used to filter and limit all received data. The data enters the ASFIC at U0201-J7. Inside U0201 the data is filtered according to data type (HS or LS), then it is limited to a 0-5V digital level. The MDC and trunking high speed data appear at U0201-G4, where it connects to the µP U0101-11

The low speed limited data output (PL, DPL, and trunking LS) appears at U0201-A4, where it connects to the µP U0101-10. While receiving low speed data, the µP may output a sampling waveform, depending on the sampling technique, to U0201-C3 between 1 and 2 kHz.

The low speed data is read by the µP at twice the frequency of the sampling waveform; a latch configuration in the ASFIC stores one bit every clock cycle. The external capacitors C0226, C0225, and C0223 set the low frequency pole for a zero crossings detector in the limiters for PL and HS data. The hysteresis of these limiters is programmed based on the type of received data. Note that during HS data the µP may generate a sampling waveform seen at U0201-G1.

## 7.2 Alert Tone Circuits

When the software determines that it needs to give the operator an audible feedback (for a good key press, or for a bad key press), or radio status (trunked system busy, phone call, circuit failures), it sends an alert tone to the speaker.

It does so by sending SPI BUS data to U0201 which sets up the audio path to the speaker for alert tones. The alert tone itself can be generated in one of two ways: internally by the ASFIC, or externally using the µP and the ASFIC.

The allowable internal alert tones are 304, 608, 911, and 1823Hz. In this case a code contained within the SPI BUS load to the ASFIC sets up the path and determines the tone frequency, and at what volume level to generate the tone. (It does not have to be related to the voice volume setting).

For external alert tones, the μP can generate any tone within the 100-3000Hz audio band. This is accomplished by the μP generating a square wave which enters the ASFIC at U0201-C3.

Inside the ASFIC, this signal is routed to the alert tone generator. The output of the generator is summed into the audio chain just after the RX audio de-emphasis block. Inside U0201 the tone is amplified and filtered, then passed through the 8-bit digital volume attenuator, which is typically loaded with a special value for alert tone audio. The tone exits at U0201-J4 and is routed to the audio PA like receive audio.

# UHF (403-470MHz) SPECIFIC CIRCUIT DESCRIPTION

## 8.0 Receiver Front-End

The receiver is able to cover the UHF range from 403 to 470 MHz. It consists of four major blocks: front-end, mixer, first IF section and IF IC. Antenna signal pre-selection is performed by two varactor tuned bandpass filters. A double balanced shottky diode mixer converts the signal to the first IF at 45.1 MHz.

Two crystal filters in the first IF section and two ceramic filters in the second IF section provide the required selectivity. The second IF at 455 kHz is mixed, amplified and demodulated in the IF IC. The processing of the demodulated audio signal is performed by an audio processing IC located in the controller section.

### 8.1 Front-End Band-Pass Filter & Pre-Amplifier

A two pole pre-selector filter tuned by the varactor diodes D5301 and D5302 pre-selects the incoming signal (PA RX) from the antenna switch to reduce spurious effects to following stages. The tuning voltage (FE CNTL VLTG) ranging from 2 volts to 8 volts is controlled by a Digital to Analogue (D/A) converter (U0731-11) in the controller section. A dual hot carrier diode (D5303) limits any inband signal to 0 dBm to prevent damage to the pre-amplifier.

The RF pre-amplifier is an SMD device (Q5301) with collector base feedback to stabilize gain, impedance, and intermodulation. The collector current of approximately 11-16 mA is drawn from the voltage 9V3 via L5302 and R5302. A 3dB pad (R5306 - R5308 and R5317 - R5319) stabilizes the output impedance and intermodulation performance.

A second two pole varactor tuned bandpass filter provides additional filtering to the amplified signal. The varactor diodes D5304 and D5305 are controlled by the same signal which controls the pre-selector filter. A following 1 dB pad (R5310, R5314, R5316) stabilizes the output impedance and intermodulation performance

If the UHF radio is configured for a base station application, R5319 is not placed and TP5301 and TP5302 are shorted.

## 8.2 Mixer and Intermediate Frequency (IF) Section

The signal coming from the front-end is converted to the first IF (45.1 MHz) using a double balanced schottky diode mixer (D5401). Its ports are matched for incoming RF signal conversion to the 45.1MHz IF using low side injection. The injection signal (VCO MIXER) coming from the mixer buffer (Q5771) is filtered by the lowpass consisting of (L5403, L5404, C5401 - C5403) and has a level of approximately 10 dBm.

The mixer IF output signal (RX IF) from transformer T5401 pin 2 is fed to the first two pole crystal filter Y5201. The filter output in turn is matched to the following IF amplifier.

The IF amplifier Q5201 is actively biased by a collector base feedback (R5201, R5202) to a current drain of approximately 5 mA drawn from the voltage 5V STAB. Its output impedance is matched to the second two pole crystal filter Y5202. A dual hot carrier diode (D5201) limits the filter output voltage swing to reduce overdrive effects at RF input levels above -27 dBm.

## 8.3 IF IC (U5201)

The first IF signal from the crystal filters feeds the IF IC (U5201) at pin 6. Within the IF IC the 45.1MHz first IF signal mixes with the second local oscillator (LO) at 44.645MHz to the second IF at 455 kHz. The second LO uses the external crystal Y5211. The second IF signal is amplified and filtered by two external ceramic filters (FL5201, FL5202). Back in the IF IC the signal is demodulated in a phase-lock detector and fed from IF IC pin 28 to the audio processing circuit ASFIC U0201 located in the controller section (line DET AUDIO).

The squelch circuit of the IF IC is not used. Instead the squelch circuit inside the audio processing IC ASFIC (U0201) determines the squelch performance and sets the squelch threshold. The detector output signal from IF IC (U5201) pin 28 (DET_AUDIO) is fed to the ASFIC pin H7.At IF IC pin 11 an RSSI signal is available with a dynamic range of 70 dB.

The RSSI signal is interpreted by the microprocessor (U0101 pin 44) and in addition after buffering by op-amp U0202-3 available at accessory connector J0400-15.

# 9.0 Transmitter Power Amplifier (PA) 5-25W

The radio’s 5-25 W PA is a four stage amplifier used to amplify the output from the exciter to the radio transmit level. It consists of the following four stages in the line-up. The first (Q5510) is a bipolar stage that is controlled via the PA control line (line PWR CNTL). It is followed by another bipolar stage (Q5520), a MOS FET stage (Q5530) and a final bipolar stage (Q5536).

Devices Q5510 and Q5520 are surface mounted. Bipolar Transistor Q5536 and MOS FET Q5530 are directly attached to the heat sink.

## 9.1 Power Controlled Stage

The first stage (Q5510) amplifies the RF signal from the VCO (line EXCITER PA) and controls the output power of the PA. The output power of the transistor Q5510 is proportional to its collector current which is adjusted by a voltage controlled current source consisting of Q5612, Q5611 and Q5621. The whole stage operates off the K9V1 source which is 9.1V in transmit mode and nearly 0V in receive mode.

The collector current of Q5510 causes a voltage drop across the resistors R5623 and R5624. Transistor Q5612 adjusts the voltage drop across R5621 controlled through the PA control line (PWR CNTL). The current source Q5621 adjusts the collector current of Q5510 by modifying its base voltage via (R5502, L5501) until the voltage drop across R5623 and R5624 plus $V_{BE}$ (0.6V) equals the voltage drop across R5621 plus $V_{BE}$ (0.6V) of Q5611. If the voltage of PWR CNTL is raised, the base voltage of Q5612 will also rise causing more current to flow to the collector of Q5612 and a higher voltage drop across R5621. This in turn results in more current driven into the base of Q5510 by Q5621 so that the collector current of Q5510 is increased. The collector current settles when the voltage over the series configuration of R5623 and R5624 plus $V_{BE}$ (0.6V) of Q5621 equals the voltage over R5621 plus $V_{BE}$ (0.6V) of Q5611.

By controlling the output power of Q5510 and in turn the input power of the following stages the ALC loop is able to regulate the output power of the transmitter. Q5611 is used for temperature compensation of the PA output power.

In receive mode the PA control line (PWR CNTL) is at ground level and switches off the collector current of Q5612 which in turn switches off the current source transistor Q5621 and the RF transistor Q5510.

## 9.2 PA Stages

The bipolar transistor Q5520 is driven by Q5510. To reduce the collector - emitter voltage and in turn the power dissipation of Q5510 its collector current is drawn from the antenna switch circuit.

In transmit mode the base of Q5520 is slightly positive biased by a divided K9V1 signal. This bias along with the RF signal from Q5510 allows a collector current to be drawn from the antenna switch circuit and in turn switches the antenna switch to transmit, while in receive mode the low K9V1 signal with no RF signal present cuts off the collector current and in turn switches the antenna switch to receive.

The following stage uses an enhancement mode N-Channel MOS FET device (Q5530) and requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line BIAS VLTG is set in transmit mode by a Digital to Analogue (D/A) converter (U0731-4) and fed to the gate of Q5530 via the resistive network R5521, R5522 and R5523. The bias voltage is tuned in the factory. If the transistor is replaced, the bias voltage must be tuned with the Dealer Programming Software (DPS). Care must be taken, not to damage the device by exceeding the maximum allowed bias voltage. The collector current is drawn from the supply voltage A+ via L5532.

The final stage uses the bipolar device Q5536 and operates off the A+ supply voltage. For class C operation the base is DC grounded by two series inductors (L5533, L5534). A matching network consisting of C5541-C5544 and two striplines transforms the impedance to 50 Ohms and feeds the directional coupler.

## 9.3 Directional Coupler

The directional coupler is a microstrip printed circuit which couples a small amount of the forward power off the RF power from Q5536. The coupled signal is rectified to an output power proportional negative DC voltage by the diode D5553 and sent to the power control circuit in the controller section via the line PWR DETECT for output power control. The power control circuit holds this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

## 9.4 Antenna Switch

The antenna switch is switched synchronously with the K9V1 voltage and feeds either the antenna signal coming through the harmonic filter to the receiver or the transmitter signal coming from the PA to the antenna via the harmonic filter.

In transmit mode, this K9V1 voltage is high and biases Q5520 and along with the RF signal from Q5510 allows a collector current to be drawn. The collector current of Q5520 drawn from A+ flows via L5542, L5541, directional coupler, D5551, L5551, D5631, L5631, R5616, R5617 and L5611 and switches the PIN diodes D5551 and D5631 to the low impedance state. D5551 leads the RF signal from the directional coupler to the harmonic filter. The low impedance of D5631 is transformed to a high impedance at the input of the harmonic filter by the resonant circuit formed by L5551, C5633 and the input capacitance of the harmonic filter.

In receive mode the low K9V1 and no RF signal present from Q5510 turn off the collector current of Q5520. With no current drawn by Q5520 and resistor R5615 pulling the voltage at PIN diode D5631 to A+ both PIN diodes are switched to the high impedance state. The antenna signal, coming through the harmonic filter, is channelled to the receiver via L5551, C5634 and line PA RX.

A high impedance resonant circuit formed by D5551 in off state and L5554, C5559 prevents an influence of the receive signal by the PA stages. The high impedance of D5631 in off state doesn´t influence the receiver signal.

## 9.5 Harmonic Filter

The transmitter signal from the antenna switch is channelled through the harmonic filter to the antenna connector J5501.The harmonic filter is formed by inductors L5552, L5553, and capacitors C5557, C5552 through C5555. This network forms a low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R5550 is used for electro - static protection.

## 9.6 Power Control

The power control loop regulates transmitter power with an automatic level control (ALC) loop and provides protection features against excessive control voltage and high operating temperatures.

MOS FET device bias, power and control voltage limit are adjusted under microprocessor control using a Digital to Analogue (D/A) converter (U0731). The microprocessor writes the data into the D/A converter via serial interface (SRL) composed of the lines SPI CLCK SRC (clock), SPI DATA SRC (data) and DAC CE (chip enable). The D/A adjustable control voltage limit increases transmitter rise time and reduces adjacent channel splatter as it is adjusted closer to the actual operating control voltage.

The microprocessor controls K9V1 ENABLE (U0101-3) to switch on the first and the second PA stage via transistors Q0741, Q0742 and signal K9V1. The antenna switch is turned on by the collector current of the second PA stage. PA DISABLE, also microprocessor controlled (U0101-34), sets BIAS VLTG (U0731-4) and VLTG LIMIT SET (U0731-13) via Q0731, D0731 in receive mode to low to switch off the bias of the MOS FET device Q5530 and to switch off the power control voltage (PWR CNTL).

Through an Analogue to Digital (A/D) input (VLTG LIMIT) the microprocessor can read the PA control voltage (PWR CNTL) during the tuning process.

The ALC loop regulates power by adjusting the PA control line PWR CNTL to keep the forward power voltage PWR DETECT at a constant level.

Opamp U0701-2 and resistors R0701 to R0703 and R0731 subtract the negative PWR DETECT voltage from the PA PWR SET D/A output U0731 pin 2. The result is connected to opamp inverting input U0701-4 pin 9 which is compared with a 4.6 volt reference VAG present at noninverting input U0701-4 pin 10 and controls the output power of the PA via pin 8 and control line PWR CNTL. The 4.6 volt reference VAG is set by a resistive divider circuit (R0251, R0252) which is connected to ground and 9.3 volts and buffered by opamp U0251-1.

During normal transmitter operation the voltages at the opamp inputs U0701-4 pins 9 and 10 should be equal to 4.6 volts and the PA control voltage output at pin 8 should be between 4 and 7 volts. If power falls below the desired setting, PWR DETECT becomes less negative, causing the output at U0701-2 pin 7 to decrease and the opamp output U0701-4 pin 8 to increase.

A comparator formed by U0701-4 increases the PA control voltage PA CNTL until PWR DETECT is at the desired level. The power set D/A output voltage PWR SET (U0731-2) at U0701-2 pin 5 adjusts power in steps by adjusting the required value of PWR DETECT. As PA PWR SET (U0731-2) decreases, transmitter power must increase to make PWR DETECT more negative and keep the inverting input U0701-4 pin 9 at 4.6 volts.

Loop frequency response is controlled by opamp feedback components R0712 and C0711. Opamp U0701-3 compares the power control voltage PWR CNTL divided by resistors R0717 to R0719 with the voltage limit setting VLTG LIMIT SET from the D/A converter (U0731-13) and keeps the control voltage constant via Q0711 if the control voltage, reduced by the resistive divider (R0717 to R0719), approaches the voltage of VLTG LIMIT SET (U0731-13).

Rise and fall time of the output power during transmitter keying and dekeying is controlled by the comparator formed by opamp U0701-3.

During normal transmitter operation the voltage at U701-3 pin 13 is higher than the voltage at pin 12 causing the output at pin 14 being low and switching off transistor Q0711. Diode D0732 reduces the bias voltage BIAS VLTG for low control voltage levels.

The temperature of the PA area is monitored by opamp U0701-1 using thermistor R5641 (located in the PA section). If the temperature increases, the resistance of the thermistor decreases, decreasing the voltage PA TEMP. The inverting amplifier formed by U0701-1 amplifies the PA TEMP voltage and if the voltage at opamp pin 1 approaches 4.6 V plus the voltage (ON) across D0721, U701-1 simulates an increased power which in turn decreases the power control voltage until the voltage at U0701-4 pin 9 is 4.6V again. Resistor R0724, R0722, R0723 set the factor of the decrease in output power per temperature increase while R0721 through R0723 set the threshold were the temperature starts reducing the output power. During normal transmitter operation the output voltage of opamp U701-1 pin 1 is below 4.6V. Diode D5601 located in the PA section acts as protection against transients and wrong polarity of the supply voltage.

# 10.0 Frequency Synthesis

The complete synthesizer subsystem consists of the Reference Oscillator (Y5701 or U5702), the Fractional-N synthesizer (U5701), the Voltage Controlled Oscillator (Q5741), the RX and TX buffer stages (Q5751, Q5771, Q5781) and the feedback amplifier (Q5791).

## 10.1 Reference Oscillator

The Reference Oscillator (Y5702) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An Analogue to Digital (A/D) converter internal to U5701 (FRAC-N) and controlled by the microprocessor via serial interface (SRL) sets the voltage at the warp output of U5701 pin 16 to set the frequency of the oscillator. The output of the oscillator (pin 2 of Y5702) is applied to pin 14 (XTAL1) of U5701 via a RC series combination.

Some models use the Reference Oscillator U5702 instead of Y5702. The Reference Oscillator (U5702) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. This oscillator is tuned by a temperature referenced 5 bit Analogue to Digital (A/D) converter. The output of the oscillator (pin 10 of U5702) is applied to pin 14 (XTAL1) of U5701 via a RC series combination. The serial interface (SRL) for control is connected to the µP via the data line SPI DATA (U5702-25), clock line SPI CLK (U5702-22), and chip enable line PEND CE (U5702-24).

In applications were less frequency stability is required the oscillator inside U5701 is used along with an external crystal Y5701, the varactor diode D5702, C5708, C5710 and R5704. The crystal may not be replaced in case of failure. Instead of the crystal, the reference oscillator Y5702 must be soldered in along with C5706, C5707, R5703. Components Y5701, C5708, C5710, R5704, D5702 must be removed and the value of C5709 must be changed. Afterwards the radio must be retuned.

## 10.2 Fractional-N Synthesizer (U5701)

The FRAC-N synthesizer IC (U5701) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analogue modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 9.3 volts.

A voltage of 9.3V applied to the super filter input (U5701 pin 19) supplies an output voltage of 8.6 VDC at pin 18. It supplies the VCO (Q5741), VCO modulation bias circuit (via R5714) and the synthesizer charge pump resistor network (R5723, R5724, R5726). The synthesizer supply voltage is provided by the 5V regulator U5801.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U5701-32), a voltage of 13 VDC is being generated by the positive voltage multiplier circuitry (D5701-1-3, C5716, C5717). This voltage multiplier is basically a diode capacitor network driven by two (1.05MHz) 180 degrees out of phase signals (U5701-9 and -10).

Output LOCK (U5701-2) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U5701 divides the 16.8 MHz reference frequency down to 2.1 MHz and provides it at pin 11. This signal is used as clock signal by the controller.

The serial interface (SRL) is connected to the microprocessor via the data line SPI DATA (U5701-5), clock line SPI CLK (U5701-6), and chip enable line FRACN CE (U5701-7).

## 10.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) is formed by the colpitts oscillator FET Q5741. Q5741 draws a drain current of 12 mA from the FRAC-N IC super filter output. The oscillator frequency is half of the desired frequency and mainly determined by L5743, C5742, C5743, C5745 - C5748 and varactor diodes D5741 / D5742. Diode D5743 controls the amplitude of the oscillator.

A balanced frequency doubler T5751, D5751 converts the oscillator fundamental to the desired UHF frequency. With a steering voltage from 2.5V to 10.5V at the varactor diodes the full RX and TX frequency range from 357.9 MHz to 470 MHz is covered.

After the doubler a 3-pole bandpass filter rejects unwanted harmonics at the first and third oscillator fundamental frequency and matches the output to the Common VCO Buffer Q5751. Q5751 draws a collector current of 13 mA from the stabilized 5V (U5801) and drives the Pre-scaler Buffer Q5791, the PA Buffer Q5781 (Pout = 13dBm) and Mixer Buffer Q5771 (Pout = 10dBm). Q5791 draws a collector current of 8 mA from the stabilized 5V and Q5771, Q5781 both draw 17mA form the 9V3 source. The buffer stages Q5771, Q5781 and the feedback amplifier Q5791 provide the necessary gain and isolation for the synthesizer loop.

Q5731 is controlled by output AUX3 of U5701 (pin 1) and enables the RX or TX buffer. In RX mode AUX3 is nearly at ground level, in TX mode about 5V DC. In TX mode with R5732 pulled to ground level by Q5731 the modulation signal coming from the FRAC-N synthesizer IC (U5701 pin28) modulates the VCO via varactor diode D5731 while in RX mode the modulation circuit is disabled by pulling R5732 to a higher level through R5772.

## 10.4 Synthesizer Operation

The complete synthesizer subsystem works as follows. The output signal of the VCO (Q5741) is frequency doubled by doubler D5751 and, buffered by Common VCO Buffer Q5751. To close the synthesizer loop, the collector of Q5791 is connected to the PREIN port of synthesizer U5701 (pin 20). The buffer output (Q5751) also provides signals for the Mixer Buffer Q5771 and the PA Buffer (Q5781).

The pre-scaler in the synthesizer (U5701) is basically a dual modulus pre-scaler with selectable divider ratios. This divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider's output signal with the reference signal.The reference signal is generated by dividing down the signal of the reference oscillator (Y5702 or Y5701).

The output signal of the phase detector is a pulsed DC signal which is routed to the charge pump. The charge pump outputs a current at pin 29 (I OUT of U5701). The loop filter (which consists of R5715-R5717, C5723-C5725, C5727, R5741, C5741) transforms this current into a voltage that is applied to the varactor diodes D5741, D5742 and alters the output frequency of the VCO (Q5741). The current can be set to a value fixed in the FRAC-N IC or to a value determined by the currents flowing into CPBIAS 1 (U5701-27) or CPBIAS 2 (U5701-26). The currents are set by the value of R5724 or R5726 respectively. The selection of the three different bias sources is done by software programming.

To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer the magnitude of the loop current is increased by enabling the IADAPT line (U5701-31) for a certain software programmable time (Adapt Mode). The adapt mode timer is started by a low to high transient of the FRACN CE line. When the synthesizer is within the lock range the current is determined only by the resistors connected to CPBIAS 1, CPBIAS 2, or the internal current source. A settled synthesizer loop is indicated by a high level of signal LOCK DET (U5701-2).

LOCK DET adds up with signal SQ DET, weighted by resistors R0113, R0114, and is routed to one of the µP´s ADCs input U0101-43. From the voltage weighted by the resistors the µP determines whether SQ DET, LOCK DET or both are active.

In order to modulate the PLL the two spot modulation method is utilized. Via pin 8 (MODIN) on U5701 the audio signal is applied to both the A/D converter (low freq path) as well as the balance attenuator (high freq path). The A/D converter converts the low frequency analogue modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U5701-28) and connected to the VCO modulation diode D5731 via L5731, C5732.

# VHF (136-174MHz) SPECIFIC CIRCUIT DESCRIPTION

## 11.0 Receiver Front-End

The receiver is able to cover the VHF range from 136 to 174 MHz. It consists of four major blocks: front-end, mixer, first IF section and IF IC. Antenna signal pre-selection is performed by two varactor tuned bandpass filters. A double balanced schottky diode mixer converts the signal to the first IF at 45.1 MHz.

Two crystal filters in the first IF section and two ceramic filters in the second IF section provide the required selectivity. The second IF at 455 kHz is mixed, amplified and demodulated in the IF IC. The processing of the demodulated audio signal is performed by an audio processing IC located in the controller section.

### 11.1 Front-End Band-Pass Filter and Pre-Amplifier

A two pole pre-selector filter tuned by the dual varactor diode D3301 pre-selects the incoming signal (PA RX) from the antenna switch to reduce spurious effects to following stages. The tuning voltage (FE CNTL VLTG) ranging from 2 volts to 8 volts is controlled by a Digital to Analogue (D/A) converter (U0731-11) in the controller section. A dual hot carrier diode (D3303) limits any inband signal to 0dBm to prevent damage to the pre-amplifier.

The RF pre-amplifier is an SMD device (Q3301) with collector base feedback to stabilize gain, impedance, and intermodulation. The collector current of approximately 11-16 mA, drawn from the voltage 9V3 via L3302, is controlled by a current source composed of Q3302, R3302, R3300, and R3311 - R3313. In transmit mode the high K9V1 signal fed through diode D3300 switches off the current source and in turn the pre-amplifier. In receive mode K9V1 must be low to switch on the current source. A 3 dB pad (R3306 - R3308 and R3316 - R3318) stabilizes the output impedance and intermodulation performance.

A second two pole varactor tuned bandpass filter provides additional filtering to the amplified signal. The dual varactor diode D3304 is controlled by the same signal which controls the pre-selector filter.

If the radio is configured for a base station application, R3318 is not placed and TP3301 and TP3302 are shorted.

## 11.2 Mixer and Intermediate Frequency (IF) Section

The signal coming from the front-end is converted to the first IF (45.1 MHz) using a double balanced schottky diode mixer (D3331). Its ports are matched for incoming VHF signal conversion to the 45.1MHz IF using high side injection. The injection signal (VCO MIXER) coming from the mixer buffer (Q3770) is filtered by the lowpass consisting of (L3333, L3334, C3331 - C3333) and has a level of approximately 10 dBm.

The mixer IF output signal (RX IF) from transformer T3301 pin 2 is fed to the first two pole crystal filter Y5201. The filter output in turn is matched to the following IF amplifier.

The IF amplifier Q5201 is actively biased by a collector base feedback (R5201, R5202) to a current drain of approximately 5 mA drawn from the voltage 5V STAB. Its output impedance is matched to the second two pole crystal filter Y5202. A dual hot carrier diode (D5201) limits the filter output voltage swing to reduce overdrive effects at RF input levels above -27 dBm.

## 11.3 IF IC (U5201)

The first IF signal from the crystal filters feeds the IF IC (U5201) at pin 6. Within the IF IC the 45.1MHz first IF signal mixes with the second local oscillator (LO) at 44.645MHz to the second IF at 455 kHz. The second LO uses the external crystal Y5211. The second IF signal is amplified and filtered by two external ceramic filters (FL5201, FL5202). Back in the IF IC the signal is demodulated in a phase-lock detector and fed from IF IC pin 28 to the audio processing circuit ASFIC U0201 located in the controller section (line DET AUDIO).

The squelch circuit of the IF IC is not used. Instead the squelch circuit inside the audio processing IC ASFIC (U0201) determines the squelch performance and sets the squelch threshold. The detector output signal from IF IC (U5201) pin 28 (DET AUDIO) is fed to the ASFIC pin H7.

At IF IC pin 11 an RSSI signal is available with a dynamic range of 70 dB. The RSSI signal is interpreted by the microprocessor (U0101 pin 44) and in addition after buffering by op-amp U0202-3 available at accessory connector J0400-15.

# 12.0 Transmitter Power Amplifier (PA) 5-25W

The radio’s 5-25 W PA is a three stage amplifier used to amplify the output from the exciter to the radio transmit level. It consists of the following stages in the line-up. The first (Q3511) is a bipolar stage that is controlled via the PA control line (line PWR CNTL). It is followed by a MOS FET stage (Q3521) and a final bipolar stage (Q3531). Devices Q3511 and Q3521 are surface mounted. Bipolar Transistor Q3531 is directly attached to the heat sink.

## 12.1 Power Controlled Stage

The first stage (Q3511) amplifies the RF signal from the VCO (line EXCITER PA) and controls the output power of the PA. The output power of the transistor Q3511 is proportional to its collector current which is adjusted by a voltage controlled current source consisting of Q3641, (Q3643-T3 only) and Q3642. The current of the whole stage is drawn from the RX-TX Switch through coil L3652.

Transistor Q3643 (not in all models), controlled by the microprocessor via signal K9V1, switches the current source on in transmit mode and off in receive mode.

The collector current of Q3511, drawn via L3511/L3641, causes a voltage drop across the resistors R3645 and R3646. Transistor Q3641 adjusts the voltage drop across R3644 controlled through the PA control line (PWR CNTL). The current source Q3642 adjusts the collector current of Q3511 by modifying its base voltage via R3647 until the voltage drop across R3645 and R3646 plus $V_{BE}$ (0.6V) equals the voltage drop across R3644. If the voltage of PWR CNTL is raised, the base voltage of Q3641 will also rise causing more current to flow to the collector of Q3641 and a higher voltage drop across R3644. This in turn results in more current driven into the base of Q3511 by Q3642 so that the current of Q3511 is increased. The collector current settles when the voltage over the series configuration of R3645 and R3646 plus $V_{BE}$ of Q3642 equals the voltage over R3644. By controlling the output power of Q3511 and in turn the input power of the following stages the ALC loop is able to regulate the output power of the transmitter.

In receive mode the PA control line (PWR CNTL) is at ground level and switches off the collector current of Q3641 which in turn switches off the current source transistor Q3642 and the RF transistor Q3511.

## 12.2 PA Stages

The following stage uses an enhancement mode N-Channel MOS FET device (Q3521) and requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line BIAS VLTG is set in transmit mode by a Digital to Analogue (D/A) converter (U0731-4) and fed to the gate of Q3521 via the resistive network R3613, R3614, R3615. The bias voltage is tuned in the factory. If the transistor is replaced, the bias voltage must be tuned with the Dealer Programming Software (DPS). Care must be taken, not to damage the device by exceeding the maximum allowed bias voltage. The collector current is drawn from the supply voltage A+ via L3622.

The final stage uses the bipolar device Q3531 and operates off the A+ supply voltage. For class C operation the base is DC grounded by two series inductors (L3521, L3522). A matching network consisting of C3530-C3534, L3532, L3533 and two striplines transforms the impedance to 50 Ohms and feeds the directional coupler.

## 12.3 Directional Coupler

The directional coupler is a microstrip printed circuit which couples a small amount of the forward power off the RF power from Q3531. The coupled signal is rectified to an output power proportional negative DC voltage by the diode D3657 and sent to the power control circuit in the controller section via the line PWR DETECT for output power control. The power control circuit holds this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

## 12.4 Antenna Switch

The antenna switch is switched synchronously with the K9V1 voltage along with the voltage PWR CNTL signal and feeds either the antenna signal coming through the harmonic filter to the receiver or the transmitter signal coming from the PA to the antenna via the harmonic filter.

In transmit mode, this PWR CNTL is above 1 V and biases Q3511 through Q3641 and Q3642 to allow a collector current to be drawn. The collector current of Q3511 drawn from A+ flows via L3631, L3531, L3532, L3533, directional coupler, D3551, L3651, D3651, L3652, R3645, R3646, L3641, L3511 and switches the PIN diodes D3551 and D3651 to the low impedance state. D3551 leads the RF signal from the directional coupler to the harmonic filter. The low impedance of D3651 is transformed to a high impedance at the input of the harmonic filter by the resonant circuit formed by L3651,C3652 and the input capacitance of the harmonic filter.

Transistor Q3643, controlled by the microprocessor via Signal K9V1, is used to switch the collector current of Q3641 on in transmit mode and off in receive mode. In receive mode the low K9V1 and the low PWR CNTL turn off the collector current of Q3511 through Q3641 and Q3642. With no current drawn by Q3511 and resistor R3651 pulling the voltage at PIN diode D3651 to A+ both PIN diodes are switched to the high impedance state. The antenna signal, coming through the harmonic filter, is channelled to the receiver via L3651, C3651 and line PA RX. The high impedance of D3551/ D3651 in off state does not influence the receiver signal.

## 12.5 Harmonic Filter

The transmitter signal from the antenna switch is channelled through the harmonic filter to the antenna connector J3501.The harmonic filter is formed by inductors L3551, L3552, and capacitors C3551 through to C3554 This network forms a low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R3551 is used for electro-static protection.

## 12.6 Power Control

The power control loop regulates transmitter power with an automatic level control (ALC) loop and provides protection features against excessive control voltage and high operating temperatures.

MOS FET device bias, power and control voltage limit are adjusted under microprocessor control using a Digital to Analogue (D/A) converter (U0731). The microprocessor writes the data into the D/ A converter via serial interface (SRL) composed of the lines SPI CLCK SRC (clock), SPI DATA SRC (data) and DAC CE (chip enable). The D/A adjustable control voltage limit increases transmitter rise time and reduces adjacent channel splatter as it is adjusted closer to the actual operating control voltage.

The microprocessor controls K9V1 ENABLE (U0101-3) to switch on the first PA stage via transistors Q0741, Q0742 and signal K9V1. The antenna switch is turned on by the collector current of the first PA stage. PA DISABLE, also microprocessor controlled (U0101-34), sets BIAS VLTG (U0731-4) and VLTG LIMIT SET (U0731-13) via Q0731, D0731 in receive mode to low to switch off the bias of the MOS FET device Q3521 and to switch off the power control voltage (PWR CNTL).

Through an Analogue to Digital (A/D) input (VLTG LIMIT) the microprocessor can read the PA control voltage (PWR CNTL) during the tuning process.

The ALC loop regulates power by adjusting the PA control line PWR CNTL to keep the forward power voltage PWR DETECT at a constant level.

Opamp U0701-2 and resistors R0701 to R0703 and R0731 subtract the negative PWR DETECT voltage from the PA PWR SET D/A output U0731 pin 2. The result is connected to opamp inverting input U0701-4 pin 9 which is compared with a 4.6 volt reference VAG present at noninverting input U0701-4 pin 10 and controls the output power of the PA via pin 8 and control line PWR CNTL. The 4.6 volt reference VAG is set by a resistive divider circuit (R0251, R0252) which is connected to ground and 9.3 volts and buffered by opamp U0251-1.

During normal transmitter operation the voltages at the opamp inputs U0701-4 pins 9 and 10 should be equal to 4.6 volts and the PA control voltage output at pin 8 should be between 4 and 7 volts. If power falls below the desired setting, PWR DETECT becomes less negative, causing the output at U0701-2 pin 7 to decrease and the opamp output U0701-4 pin 8 to increase.

A comparator formed by U0701-4 increases the PA control voltage PA CNTL until PWR DETECT is at the desired level. The power set D/A output voltage PWR SET (U0731-2) at U0701-2 pin 5 adjusts power in steps by adjusting the required value of PWR DETECT. As PWR SET (U0731-2) decreases, transmitter power must increase to make PWR DETECT becomes more negative and keep the inverting input U0701-4 pin 9 at 4.6 volts.

Loop frequency response is controlled by opamp feedback components R0712 and C0711. Opamp U0701-3 compares the power control voltage PWR CNTL divided by resistors R0717 to R0719 with the voltage limit setting VLTG LIMIT SET from the D/A converter (U0731-13) and keeps the control voltage constant via Q0711 if the control voltage, reduced by the resistive divider (R0717 to R0719), approaches the voltage of VLTG LIMIT SET (U0731-13).

Rise and fall time of the output power during transmitter keying and dekeying is controlled by the comparator formed by opamp U0701-3.

During normal transmitter operation the voltage at U701-3 pin 13 is higher than the voltage at pin 12 causing the output at pin 14 being low and switching off transistor Q0711. Diode D0732 reduces the bias voltage BIAS VLTG for low control voltage levels.

The temperature of the PA area is monitored by opamp U0701-1 using thermistor R3611 (located in the PA section). If the temperature increases, the resistance of the thermistor decreases, decreasing the voltage PA TEMP. The inverting amplifier formed by U0701-1 amplifies the PA TEMP voltage and if the voltage at opamp pin 1 approaches 4.6 V plus the voltage (ON) across D0721, U701-1 simulates an increased power which in turn decreases the power control voltage until the voltage at U0701-4 pin 9 is 4.6V again. Resistor R0724, R0722, R0723 set the factor of the decrease in output power per temperature increase while R0721 through R0723 set the threshold were the temperature starts reducing the output power. During normal transmitter operation the output voltage of opamp U701-1 pin 1 is below 4.6V. Diode D3601 located in the PA section acts as protection against transients and wrong polarity of the supply voltage.

# 13.0 Frequency Synthesis

The complete synthesizer subsystem consists of the Reference Oscillator (Y3701 or Y3702), the Fractional-N synthesizer (U3701), the Voltage Controlled Oscillator (Q3741, Q3751), the RX and TX buffer stages (Q3760, Q3770, Q3780) and the feedback amplifier (Q3790).

## 13.1 Reference Oscillator

The Reference Oscillator (Y3702) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An Analogue to Digital (A/D) converter internal to U3701 and controlled by the microprocessor via serial interface (SRL) sets the voltage at the warp output of U3701 pin 16 to set the frequency of the oscillator. The output of the oscillator (pin 2 of Y3702) is applied to pin 14 (XTAL1) of U3701 via a RC series combination.

In applications were less frequency stability is required the oscillator inside U3701 is used along with an external crystal Y3701, the varactor diode D3702, C3708, C3710 and R3704. The crystal may not be replaced in case of failure. Instead of the crystal, the reference oscillator Y3702 must be soldered in along with C3706, C3707, R3703. Components Y3701, C3708, C3710, R3704, D3702 must be removed and the value of C3709 must be changed. Afterwords the radio must be retuned.

## 13.2 Fractional-N Synthesizer (U3701)

The FRAC-N synthesizer IC (U3701) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analogue modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 9.3 volts.

A voltage of 9.3V applied to the super filter input (U3701 pin 19) supplies an output voltage of 8.6 VDC at pin 18. It supplies the VCO (Q3741 / Q3751), VCO modulation bias circuit (R3714) and the synthesizer charge pump resistor network (R3723, R3724). The synthesizer supply voltage is provided by the 5V regulator U3801.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U3701-32), a voltage of 13 VDC is being generated by the positive voltage multiplier circuitry (D3701-1-3, C3716, C3717). This voltage multiplier is basically a diode capacitor network driven by two (1.05 MHz) 180 degrees out of phase signals (U3701-9 and -10).

Output LOCK (U3701-2) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U3701 divides the 16.8 MHz reference frequency down to 2.1 MHz and provides it at pin 11. This signal is used as clock signal by the controller.

The serial interface (SRL) is connected to the microprocessor via the data line SPI DATA (U3701-5), clock line SPI CLK (U3701-6), and chip enable line FRACN CE (U3701-7).

## 13.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) uses 2 colpitts oscillators, FET Q3741 for transmit and FET Q3751 for receive. The appropriate oscillator is switched on or off by FRAC-N IC output AUX3 (U3701-1) using transistors Q3742 and Q3752. In RX mode AUX3 is nearly at ground level and Q3742 enables a current flow from the source of FET Q3751 while Q3752 is switched off.

In TX mode AUX3 is about 5V DC and Q3742 is switched off. Q3752 is switched on and enables a current flow from the source of FET Q3741 while Q3751 is switched off. When switched on the FETs draw a drain current of 8 mA from the FRAC-N IC super filter output. The frequency of the receive oscillator is mainly determined by L3752, C3752, C3754 - C3756 and varactor diodes D3751 / D3752. Diode D3754 controls the amplitude of the oscillator. The frequency of the transmit oscillator is mainly determined by L3734, C3736 - C3740 and varactor diodes D3732 / D3733. Diode D3739 controls the amplitude of the oscillator. With a steering voltage from 3V to 10V at the varactor diodes the RX frequency range from 181.1MHz to 219.1MHz and the TX frequency range from 136MHz to 174MHz are covered. In TX mode the modulation signal coming from the FRAC-N synthesizer IC (U3701 pin 28) modulates the TX VCO via varactor diode D3731.

Both oscillator outputs are combined and buffered by the VCO Buffer Q3760. Q3760 draws a collector current of 13 mA from the stabilized 5V (U3801) and drives the Mixer Buffer Q3770. Q3770 draws a collector current of 17 mA from the 9V3 voltage and drives the PA Buffer Q3780 (Pout = 13dBm) and the Pre-scaler Buffer Q3790. Q3790 draws a collector current of 8 mA from the stabilized 5V (U3801) and drives the pre-scaler internal to the FRAC-N IC. In transmit mode Q3780 is switched on by the K9V1 signal and draws a collector current of 19 mA from the K9V1 voltage. The injection signal VCO MIXER with a level of 10dBm feeds the mixer through R3774. The buffer stages Q3760, Q3770, Q3780 and the feedback amplifier Q3790 provide the necessary gain and isolation for the synthesizer loop.

## 13.4 Synthesizer Operation

The complete synthesizer subsystem works as follows. The combined output signal of the RX VCO (Q3751) and TX VCO (Q3741) is buffered by VCO Buffer Q3760, Mixer Buffer Q3770 and Pre-scaler Buffer Q3790. To close the synthesizer loop, the collector of Q3790 is connected to the PREIN port of synthesizer U3701 (pin 20). The output of the VCO Buffer (Q3770) also provides signals for the mixer (via VCO MIXER) and the PA Buffer (Q3780).

The pre-scaler in the synthesizer (U3701) is basically a dual modulus pre-scaler with selectable divider ratios. This divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider´s output signal with the reference signal.The reference signal is generated by dividing down the signal of the reference oscillator (Y3701 or Y3702).

The output signal of the phase detector is a pulsed DC signal which is routed to the charge pump. The charge pump outputs a current at pin 29 (I OUT of U3701). The loop filter (which consists of R3715 - R3718, C3723 - C3725, C3727, C3735) transforms this current into a voltage that is applied to the varactor diodes D3732, D3733 (TX), D3751, D3752 (RX) and alters the output frequency of the TX VCO (Q3741) and RX VCO (Q3751). The current can be set to a value fixed in the FRAC-N IC or to a value determined by the current flowing into CPBIAS 1 (U3701-27). The current is set by the value of R3723 and R3724. The selection of the two different bias sources is done by software programming.

To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer the magnitude of the loop current is increased by enabling the IADAPT line (U3701-31) for a certain software programmable time (Adapt Mode). The adapt mode timer is started by a low to high transient of the FRACN CE line. When the synthesizer is within the lock range the current is determined only by the resistors connected to CPBIAS 1 or the internal current source.

A settled synthesizer loop is indicated by a high level of signal LOCK DET (U3701-2).

LOCK DET adds up with signal SQ DET, weighted by resistors R0113, R0114, and is routed to one of the µP´s ADCs input U0101-43. From the voltage weighted by the resistors the µP determines whether SQ DET, LOCK DET or both are active.

In order to modulate the PLL the two spot modulation method is utilized. Via pin 8 (MODIN) on U3701 the audio signal is applied to both the A/D converter (low freq path) as well as the balance attenuator (high freq path). The A/D converter converts the low frequency analogue modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U3701-28) and connected to the VCO modulation diode D3731 via L3731, C3733.

# Chapter 3.2

## PCB/Schematic Diagrams and Parts Lists

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